http://www.jctjournals.com ISSN(ONLINE):2278 – 3814

Volume-8, Issue-1, January, 2019
JOURNAL OF COMPUTING TECHNOLOGIES (JCT)
International Journal
Impact Factor: 3.017

Performance Analysis of CC-Multilevel Inverter in PV System

Jyoti Patel[1], Dr. Anula Khare[2]
[1]*Research Scholar of Power Electronics*[2] *Professors*
Technocrats Institute of Technology, Bhopal MP, India
[1]jyotipatel007511@gmail.com, [2]anulakhare03@gmail.com

***Abstract*— A lot of research has been carried out to make renewable resources more efficient and easier to use. The use of photovoltaic cells in the last few days has been one of the greatest researches. PV cell generate power in DC form. A DC/AC converter is utilising to convert the DC power into AC power. So the interest of the different power converter is now becomes more popular for conversion. In this paper discuss the different work associated in the field of the power converter which is applicable in the power modulator. Also discuss the basic problems which are facing in the power converter industry.**

***Keywords*— REC, UPS, THD, MLI, DC/AC, PWM, etc.**

I. INTRODUCTION

DC / AC inverter has recently become an important device, and its pertaining relevance to many industrial, commercial and domestic applications including adjustable speed drives, renewable energy conversion system (RES), Uninterrupted Power Supplies (UPS) [1]. The inverter systems should be in low total harmonic distortion (THD), high efficiency, simplicity and low cost for these applications. Furthermore, the inverters should operate without interruption on a continuous basis. Many literature surveys are proposed with many DC / AC inverter topologies and control methods including conventional 3-level PWM DC / AC inverters, VSI voltage source inverter and CSI and ISI, as well as conventional MLI topologies.

The main disadvantage of the PWM inverting system is the high total harmonic distortion (THD) of the output voltage and current, although traditional three-level PWM converters are reliable due to a lower number of power switches. The modulation of the power switches at higher frequencies is commonly used to reduce this. There are therefore high voltage losses at power switches [1]. This means lower THD voltages are also achieved.

Many conventional MLI topologies, such as Diode Clamped MLI (DC-MLI), Flying Capacitor MLI (FC-MLI), and Cascaded H-Bridge MLI (CHB-MLI) may achieve lower total harmonic output voltage and current distortion and at the same time reduce power loss [1]. Still effective, with a low tension on power switches and no large-scale passive filters are needed [1, 2]. However a large number of power switches and DC-link caps or isolated DC sources in order to achieve less THD are necessary for the traditional MLIs with a fundamentally low switching control.

Besides numerous extensive studies carried out with the aim of improving different aspects of the conventional multi level inverter, investigators continue to contribute to the development of newer multilevel with reduced device counting and simple control circuit topology [3]. Several research efforts have started to incorporate Switched Capacitor Circuits, which have significantly reduced the number of isolated DC input sources and the number of power switches required [4,5].

Multilevel inverter topologies with a recent switched capacitor can generate more power output levels with a small number of isolated DC sources and lower use of electricity switches than the usual ones [5]. The voltage output is multilevel, and can be generated by controlling the charging and discharging of the capacitor in the multilevel configuration of the switched-capacitor circuit board supplied from a minimum number of DC input sources [4]. However, many new multi-level converter topologies still have complex structures and control circuits that require a large number of DC connection condensers and power interrupters with the gate-drive units, protection units and cooling units that are associated with this to achieve low THD voltage. Furthermore, there may be unbalanced voltage issues in these topologies and condenser tension balancing control techniques are necessary, which is made harder if higher voltage levels are attained [4].

In the next section in discuss the work associated in the field of different type of power converter which is given by researches. Also discuss the basic problem associated in the power converter industry.

II. BACKGROUND OF MULTILEVEL INVERTER

In recent years, DC / AC inverters have been gaining huge interest. A number of references to the evolution of DC / AC inverters, such as traditional three-level PWM topologies and traditional multilevel topologies, were discussed [1]. The focus is on the inverter system, especially multi-level topology, because of its ability to generate nearly multi-level AC output with low harmonic distortion. In the next section discuss the brief review on the multilevel inverter topology and their modulation control technique.

The basic topologies such as diode clamped inverter, capacitor clamped inverter and cascaded multi-cell with separate dc sources is discussed in [6]. There will be discussion of emerging topologies such as asymmetric hybrid cells and multi-level soft-switched inverters. The most relevant control and modulation methods developed for this converter family are presented in this article: multilevel modulation of the sinusoidal pulse width, multilevel selective harmonic elimination and the modulation of the space veto. The most recent and more relevant applications such as the laminators, conveyor belts and unified power flow controls have been given special attention. A comprehensive review of AC-DC (IPQC) configurations for the three phases of improved power quality, control strategies, component selection, comparative factors, recent trends, suitability and specific applications selection is presented in [7]. It aims to present researchers, designers and applied engineers dealing with three-phase AC-DC converters with state of the art IPQC technology. Also annexed for quick reference is a classified list of some 450 research articles on IPQCs. For a grid interface, a conventional drive application, and a high-speed drive application, topologies, semiconductor losses, filter aspects, part counts, starting costs and life cycle costs are compared in [8]. An H Bridge output stage with bidirectional auxiliary switches is to report the new multilevel inverter topology in [9]. This new topology significantly reduces the number of power devices and condensers needed to implement a multi-level output. The new Topology is used for the design of a five-level inverter, with the proposed topology only involving five controlled switches, eight diodes, and two condensers. The new topology reduces the number of main power switches needed by 37.5% and does not use any diodes or condensers anymore (5 in the new one against 8 in any of the other 3 configurations).

In [10] AC-AC matrix converter is proposed in contrast to 18 IGBTs of a functionally equal conventional AC-AC matrix converter, a new three-phase AC-AC sparse matrix convertor with an energy-storage element and only 15 IGBTs is used. A three-level Z-source inverter which are new topological single-level solutions for buck-boost conversion, with all the favourable benefits of retained three-level conversion [11]. Although the current Z-source3-level inverter has been effective in achieving voltage buck-boost conversion, it uses 2 LC impedance networks and 2 isolated dc sources. A three-level buck-boost output voltage converter AC-DC-AC with Z source converter is proposed in [12]. The converter is implemented via a single network of X-formed LC impedance via a low cost front-end diode rectifier to a neutral point-clamped inverter. The inverter is controlled by a three-level output tension switch, where the medium neutral capacity is unique in tapping a wye-connected capacitive filter from the star point, located at the front diode rectification for filtering the input current. A novel PWM concept which includes conditions for NP voltage balancing is developed in [13]. The principal technical disadvantage of NP clamped (NPC) is the neutral point (NP) voltage drift. Incapable of controlling the NP tension at high modulation indices and low power factors is traditional space vector pulse width modulation (SVPWM). Virtual SVPWM (VSVPWM) is able to control the voltage of the NP under full modulation indexes. However, the modulation is more complicated than SVPWM, increasing the frequency of switching and degrading the inverter output waveforms. A dc-linking Voltage balance investigation in a one-phase diode clamped inverter made of two legs of three-stage using a passive RLC circuit is present in [14]. In the diode-clamped inverter, application of the balance circuit requires proper PWM generation, but in a balanced and unbalanced way, the modulation process is identical. No measurements or additional controls are necessary for this method of dc-link voltage balance, which ensures rapid response and low energy loss. The control by the space vector modulator technique of a Z-source neutral point clamped inverter is present in [15]. This offers several advantages, both in terms of performance and harmony. The approach adopted allows optimization and digital implementation of the Z-source system without any additional commutations. In simulation, and by experimental results from a prototype converter, the techniques proposed are demonstrated.

A three-level electric vehicle traction inverter for hybrid pulse width modulation (H-PWM) in neutral point-clamped electric vehicle (EV) is developed in [16]. The strategy proposed shows the advantages of both classical space vector PWM (SV-PWMs) and carriers based pulse width modulation (CB-PWMs). The CB-PWM calculates the working cycles for the traction inverter switches so that the calculation times are reduced and the complexity of the system is controlled. Similar to the SV-PWM-based approach, the redundancies in the switching states then balance the two dc-link condenser voltages. In addition to multiple carriers, one carrier is used for PWM that reduces computational complexity further.

In [17] presents an alternative approach to solve single-phase three-level conversion problem control and modulation applied in the electric tractors system of high-speed trains. They discusses an improved DPC method based on a deadbeat active and reactive energy prevention technology, based on the principle of the deadbeat prediction of the direct torque control of ac engines. A scheme to simultaneously decrease the Zero-Sequence Current and Common-Mode Voltage (CMV) magnitude of the system present in [18]. In order to ensure a clear

understanding of the ZSCC generation, ZSCC patterns are first analysed for modulation schemes. The proposed 3-tlevel modulation scheme is introduced on the basis of the analysis. Moreover, results are analysed and compared with the methods in place in terms of the ZSCC peak values, impact on the common-mode current (CMC), the scalability analysis for the CMI and the switching losses. Both simulation and experimentation have verified the proposed procedure. A three-level input current with continued input LC-switching based on voltage boost, which retains all the advantages of multi-level QZSI / ZSI with comparatively less numbers of passive high-power components is developed in [19]. The dc input voltage can be increased and the required 3-level ac output voltage can be provided in a single phase. The proposed inverter is discussed with a steady-state analysis in order to form a relationship between the input voltage dc and the output voltage ac of three levels. A three-level neutral-point-clamping (NPC) inverter dual modulation wave pulse width modulation (CBPWM) strategy is present in [20]. Not merely overcoming one of the major NPC inverter problems, namely the low-frequency voltage oscillation at the neutral point, this modulation approach also reduces the inverter-generated CMV voltage. The stringent theoretical derivation derives the unified task cycles in each phase and allows easy obtaining of double modulation waves based on the various optimization targets.

III. LEVEL CAPACITOR CLAMPED MLI

In 1992, Meynard and Foch proposed the capacitor clamped inverter (CCMLI) which is alternatively known as the flying capacitor. Figure 1 shows the three phase capacitor clamped three level inverter.

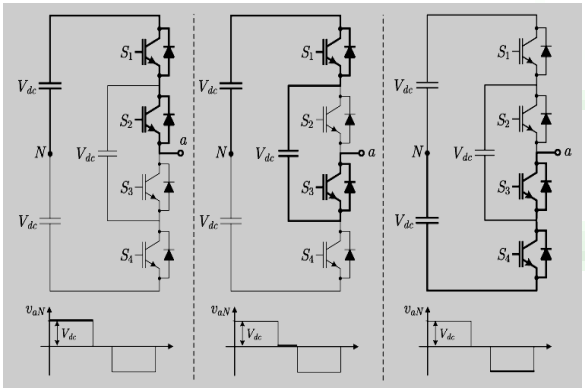

Figure 1: 3-Level Capacitor Clamped MLI

The structure of this inverter resembles that of the diode-clamped inverter, except that inverter uses capacitor instead of using clamping diodes. The flying capacitor is connected to the capacitor clamped switching cells in series. The topology consists of a dc side capacitor ladder structure, in which the voltage of the next capacitor differs on each capacitor. Two adjacent capacitor legs increase the voltage by the voltage steps in the waveform of the output.

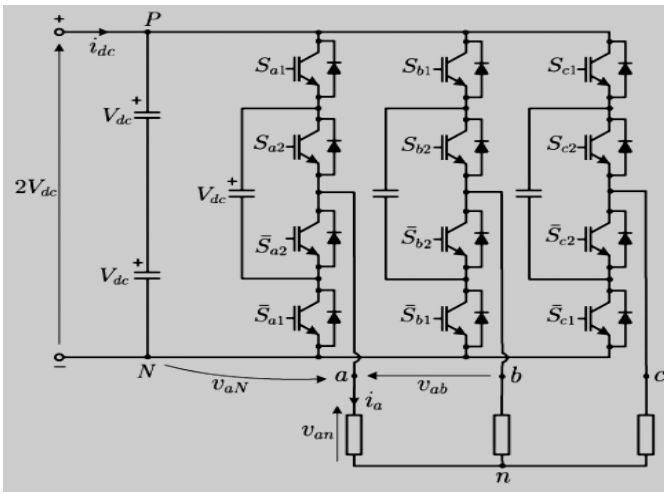

Figure 2: Switching Strategy of 3-Level CCMLI

In the operation of capacitor clamped multi-level inverter, each phase node (a, b, or c) can be connected to any node in the capacitor bank (V_3, V_2, V_1). In a three - level capacitor - clamped converter the voltage synthesis has greater flexibility than a diode - clamped converter. The following switch combinations can be synthesized using Figure 2 for the thee level CCMLI for phase –leg "a" output with respect to neutral point N (i.e. V_{an}).

Table 1: Switching State of 3-Level CCMLI with current Polarity and redundant

V_{an}	Switching State	Current Status	Conduction operation of Element	State of Capacitors
$\frac{V_{dc}}{2}$	1100	$I_a > 0$ $I_a < 0$	S_1, S_2 D_1,D_2	Uncharged Uncharged
0	1010	$I_a > 0$ $I_a < 0$	S_1,C_1,D_3 S_1',C_1,D_1	Charge C_1 Discharge C_1
0	0101	$I_a > 0$ $I_a < 0$	D_4, C_1, S_2 S_2',C_1,D_2	Discharge C_1 Charge C_1
$-\frac{V_{dc}}{2}$	0011	$I_a > 0$ $I_a < 0$	D_3, D_4 S_3, S_4	Uncharged Uncharged

Table 1 shows the basic switching state of the single leg of phase "a" of proposed three phase capacitor clamped multilevel inverter. From Table 5.1, when phase "a" output

is connected to 0, the imbalance voltage signal of a CC-MLI at 3 levels is generated. The capacitor C1 loads and discharges depending on current of phase "a" status (Ia) in switching states 1010 and 0101. The result could therefore be that the voltage balance of capacitor C1 can be maintained through proper control of the redundant switching states and phase current polarity.

IV. PV ENERGY SYSTEM

The circuit of the solar cell model, which consists of a photocurrent, diode, parallel resistor (leakage current) and a series resistor; is shown in Figure 1. According figure by the Kirchhoff's circuit laws, the photovoltaic current can be presented as follows:

[1]

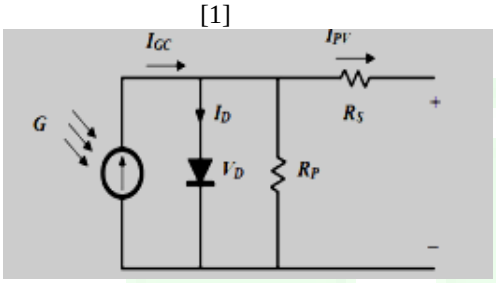

Figure 3: Electrical Equivalent Model of PV Cell

$$I_{PV} = I_{gc} - I_0\left[esp^{\left(\frac{eV_d}{KFT_c}\right)} - 1\right] - \frac{V_d}{R_P}$$

Where, I_{PV} is photovoltaic current, I_{gc} is light Generated current, I_0 is the dark saturation current, V_d is the diode voltage, K is the Boltzmann's Constant, T_c is the cell temperature, F is cell idealizing temperature, R_P is parallel resistance.

The method of perturbation and observation (P&O) is mostly utilized by other means because it is straightforward and cheaper in cost for consumer side. The pitching of the PV curve of the solar module is based on this algorithm. The voltage is disrupted in this algorithm and the slope (dP / dV) is checked for positive, negative and zero conditions. If the slope is zero, then the point is MPP, but if the slope is negative, the voltage is disrupted, and the voltage is disrupted in the back direction.

V. SIMULATION & RESULT

The proposed system is modelled in two stages stand-alone PV system with voltage is boosted with DC/DC Converter and then DC/AC converter. The P & O based MPPT technique is used for tracking in maximum power of the solar system. The output of the boost converter is now fed to the proposed CC-MLI for finding the AC output of the system. Figure 4 shows the SIMULINK model of the proposed block diagram.

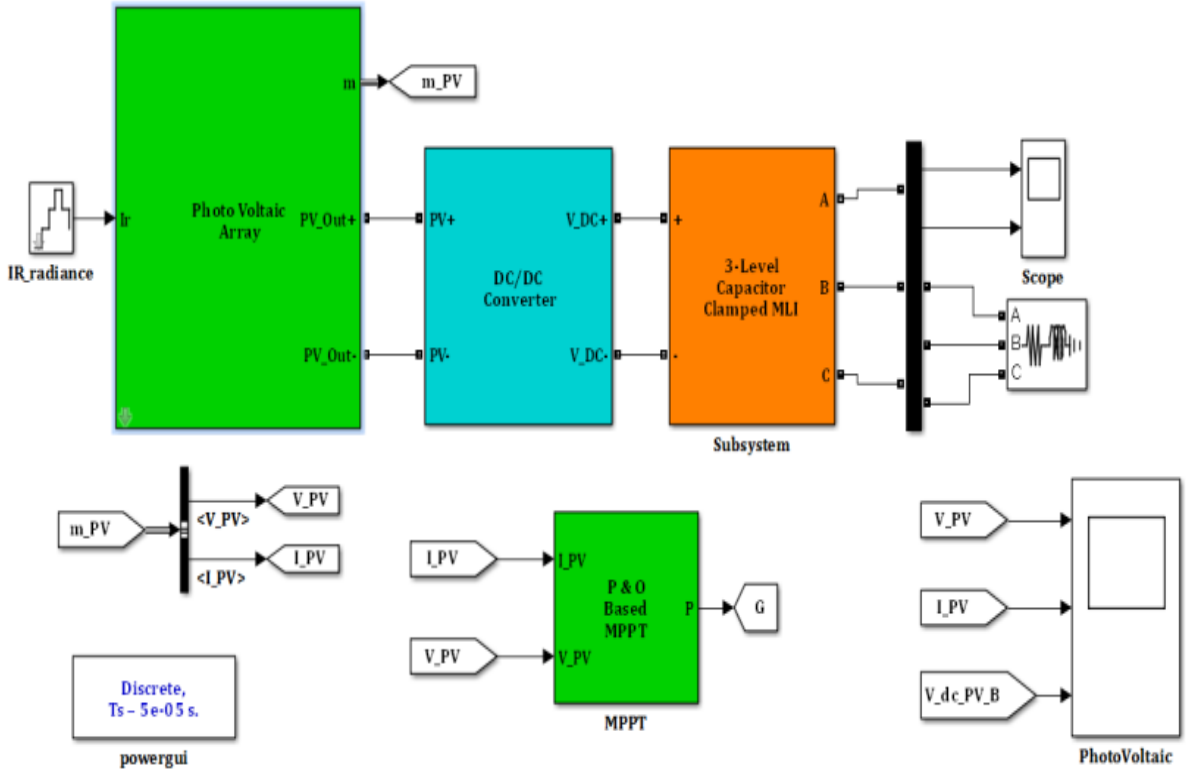

Figure 4: SIMULINK model of CC-MLI Based PV System

Table 2: Parameter of Solar Panel BP SX 3190W

Parameter of BP SX 3190W	Value
Maximum Power (P_{max})	190W_P
Minimum Power (P_{min})	172.9 W_P
Voltage at P_{max} (V_{mp})	24.3 V
Current at P_{max} (I_{mp})	7.282A
Short Circuit Current (I_{sc})	8.5 A
Open-Circuit Voltage (V_{oc})	3.6 V
Number of Cell per Module	50
Number of Series-connected Modules per string	6
Number of Parallel Strings	18
Series Resistance (R_s) , and Parallel Resistance(R_{ph})	0.175, 755.51
Saturated current (I_{sat})	1µA
Phase Current (I_{ph})	8.52 A
Load	1kW

The whole work is simulated in MATLAB software to validate the system. For designing solar system here in this work uses polycrystalline BP solar panel SX 3190W model for simulation. Table 2 shows the custom data of the solar panel BP SX 3190W a very easily available in Indian market. Figure 5 and 6 shows the I-V and P-V characteristics of the BP SX 3190W solar Panel which is used in this simulation. In figure 6.8 the circle is marked for tracking the maximum power of the BP SX 3190W solar panel.

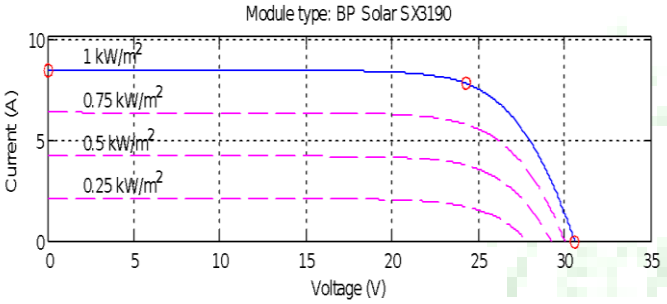

Figure 5: I-V Characteristics of one module of BP SX 3190W solar Panel

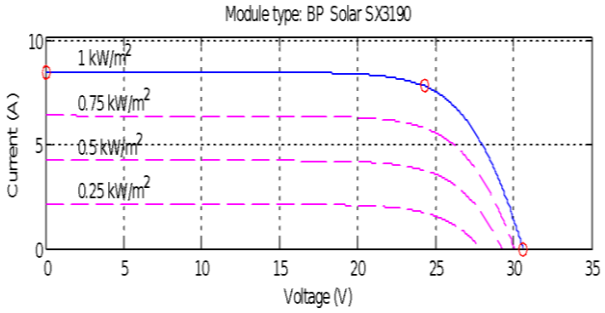

Figure 6: P-V characteristics of one module of the BP SX 3190W solar panel.

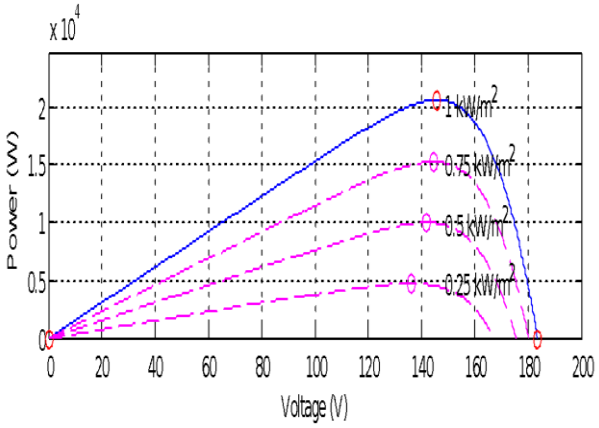

Figure 7: I-V Characteristics of an Array of the BP SX 3190W solar Panel

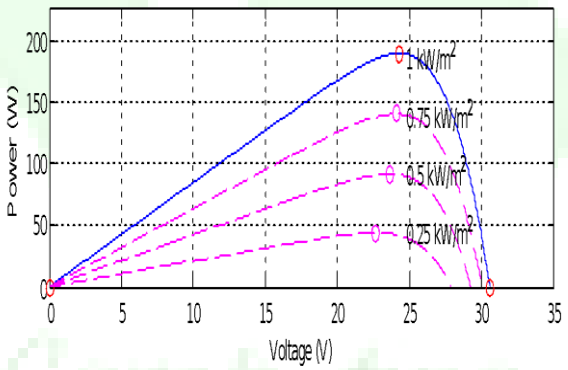

Figure 8: P-V Characteristics of an Array of the BP SX 3190W solar Pane

Figure 7 and 8 shows the array performance of the BP SX 3190W solar Panel. The Array of the panel consists of 6 series and 18 parallel strings in this. The circular mark in figure 8 shows the maximum power point of the panel. Figure 8 show the output average voltage for Jan to Dec of the year 2018. The variation of the solar irradiation is based on bimonthly data of the synergy official site.

Figure 9 and 10 shows the solar output peak voltage during the day time with the different irradiation. Figure 10 is the output voltage after boost converter which is using the MPPT based operation. Here the boost voltage is seen that it is approx to 380 V. figure 11 shows the output of the 3-level CCMLI system which is used for the conversion of the DC/AC power.

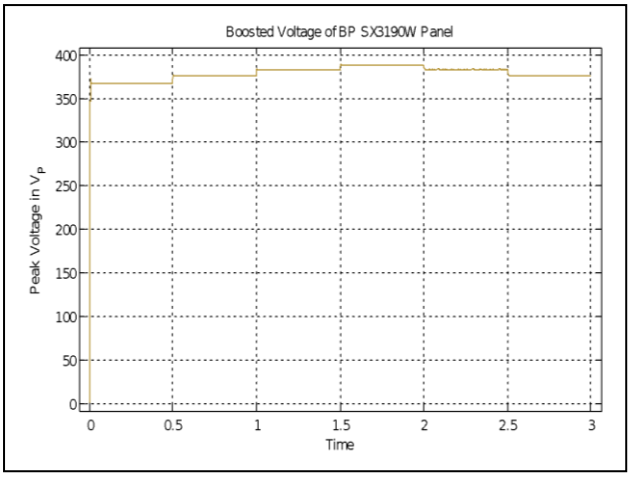

Figure 9: Peak voltage variation in day time of the BP SX 3190W solar Panel

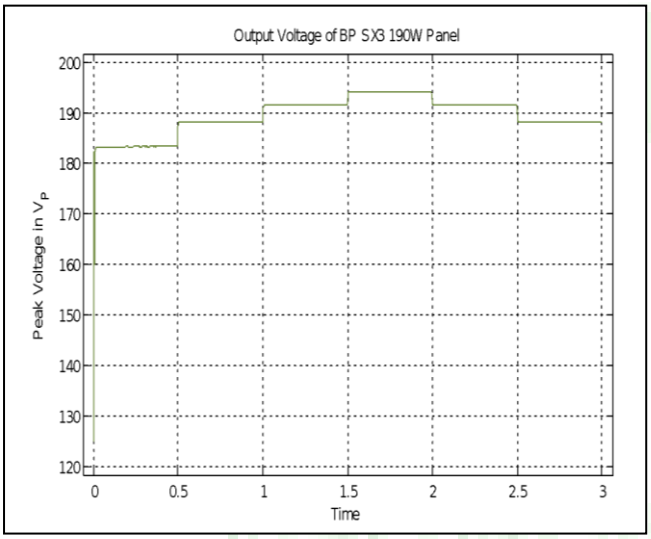

Figure 10: Peak voltage variation after boost converter for BP SX 3190 W solar Panel

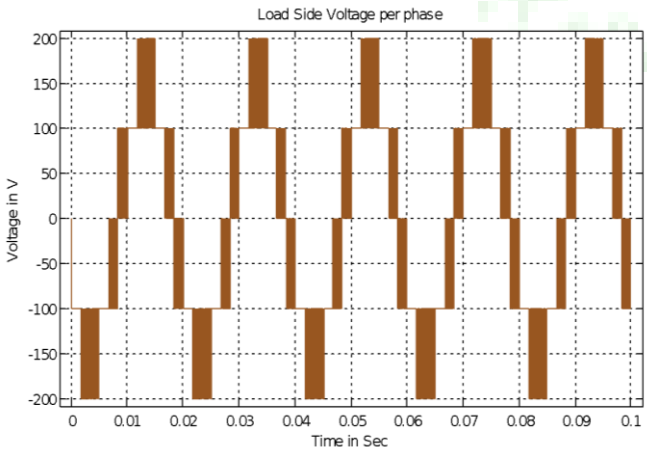

Figure 11: Load side per phase voltage of CCMLI

VI. CONCLUSIONS

This paper is based on the implementation of 3-Level Capacitor clamped multilevel inverter topology on the conventional PV system to increase the system efficiency. Here in this paper discuss the various works in the field of the multilevel inverter. Also discuss the working and the construction of capacitor clamped multi-level inverter. The CCMLI is implemented on the P & O method based conventional PV system. The whole work is simulated in MATLAB software to validate the result.

REFERENCES

[1]. A. Silva 2013, "Advanced DC/AC Inverters: Applications in Renewable Energy [Book News]", IEEE Industrial Electronics Magazine, vol. 7, no. 4, pp. 68-69.

[2]. Mecke, R. 2011, "Multilevel NPC inverter for low-voltage applications", Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on, pp. 1.

[3]. K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu & S. Jain 2016, "Multilevel Inverter Topologies With Reduced Device Count: A Review", IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 135-151.

[4]. Babaei & S. S. Gowgani 2014, "Hybrid Multilevel Inverter Using Switched Capacitor Units", IEEE Transactions on Industrial Electronics, vol. 61, no. 9, pp. 4614-4621.

[5]. Barzegarkhoo, H. M. Kojabadi, E. Zamiry, N. Vosoughi & L. Chang 2016, "Generalized Structure for a Single Phase Switched-Capacitor Multilevel Inverter Using a New Multiple DC Link Producer With Reduced Number of Switches", IEEE Transactions on Power Electronics, vol. 31, no. 8, pp. 5604-5617.

[6]. José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications", IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 4, AUGUST 2002

[7]. B. Singh ; B.N. Singh ; A. Chandra ; K. Al-Haddad ; A. Pandey ; D.P. Kothar, 2004 "A review of three-phase improved power quality AC-DC converters", IEEE Transactions on Industrial Electronics Volume: 51 , Issue: 3

[8]. R. Teichmann ; S. Bernet, 2005 "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications", IEEE Transactions on Industry Applications, Volume: 41 , Issue: 3

[9]. G. Ceglia ; V. Guzman ; C. Sanchez ; F. Ibanez ; J. Walter ; M.I. Gimenez, 2006 "A New Simplified Multilevel Inverter Topology for DC–AC Conversion", IEEE Transactions on Power Electronics,Volume: 21 , Issue: 5

[10]. Johann W. Kolar ; Frank Schafmeister ; Simon D. Round ; Hans Ertl 2007,"Novel Three-Phase AC–AC

Sparse Matrix Converters", IEEE Transactions on Power Electronics, Volume: 22 , Issue: 5
[11]. Poh Chiang Loh ; Sok Wei Lim ; Feng Gao ; Frede Blaabjerg 2007 "Three-Level Z-Source Inverters Using a Single LC Impedance Network 4", IEEE Transactions on Power Electronics,Volume: 22 , Issue: 2
[12]. Poh Chiang Loh ; Feng Gao ; Pee-Chin Tan ; Frede Blaabjerg 2009, "Three-Level AC–DC–AC Z-Source Converter Using Reduced Passive Component Count",IEEE Transactions on Power Electronics, Volume: 24 , Issue: 7
[13]. Wei-dong Jiang ; Shao-wu Du ; Liu-chen Chang ; Yi Zhang ; Qin Zhao,2010,"Hybrid PWM Strategy of SVPWM and VSVPWM for NPC Three-Level Voltage-Source Inverter", EEE Transactions on Power Electronics,Volume: 25 , Issue: 10
[14]. Robert Stala, 2011 "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs",IEEE Transactions on Industrial Electronics, Volume: 58 , Issue: 9
[15]. Francis Boafo Effah ; Patrick Wheeler ; Jon Clare ; Alan Watson, 2013, "Space-Vector-Modulated Three-Level Inverters With a Single Z-Source Network", IEEE Transactions on Power Electronics, Volume: 28 , Issue: 6
[16]. Abhijit Choudhury ; Pragasen Pillay ; Sheldon S. Williamson, 2015 "A Hybrid PWM-Based DC-Link Voltage Balancing Algorithm for a Three-Level NPC DC/AC Traction Inverter Drive", IEEE Journal of Emerging and Selected Topics in Power Electronics, Volume: 3 , Issue: 3
[17]. Wensheng Song ; Junpeng Ma ; Liang Zhou ; Xiaoyun Feng, 2016, "Deadbeat Predictive Power Control of Single-Phase Three-Level Neutral-Point-Clamped Converters Using Space-Vector Modulation for Electric Railway Traction",IEEE Transactions on Power Electronics, Volume: 31 , Issue: 1
[18]. Zhongyi Quan ; Yun Wei Li, 2017, "A Three-Level Space Vector Modulation Scheme for Paralleled Converters to Reduce Circulating Current and Common-Mode Voltage", IEEE Transactions on Power Electronics, Volume: 32 , Issue: 1
[19]. Manoranjan Sahoo ; Sivakumar Keerthipati, 2017, "A Three-Level LC-Switching-Based Voltage Boost NPC Inverter", IEEE Transactions on Industrial Electronics, Volume: 64 , Issue: 4 ,
[20]. Peng Liu ; Shanxu Duan ; Chuan Yao ; Changsong Chen, 2018 "A Double Modulation Wave CBPWM Strategy Providing Neutral-Point Voltage Oscillation Elimination and CMV Reduction for Three-Level NPC Inverters", IEEE Transactions on Industrial Electronics, Volume: 65 , Issue: 1

