Volume-8, Issue-11, November, 2019
JOURNAL OF COMPUTING TECHNOLOGIES (JCT)
International Journal
Impact Factor: 3.017

A LITERATURE SURVEY ON FPGA IMPLEMENTATION OF SPATIAL FILTERING 2D IMAGES

[1] *Pradeep kumar Chaturvedi*, (M.Tech Scholar), [2]Prof. Santosh Onkar (HOD)
[1]M.Tech Scholar- VLSI, [2]Asst. Professor
Department of Electronics & Communication Engineering
SAM College of Engineering & Technology, Bhopal, (M. P.), India
pradeepjnct2012@gmil.com

***Abstract*— In this survey paper focus on the different A Literature Survey FPGA Implementation Of Spatial Filtering 2D Images. In the current generation Spatial Filtering 2D Images plug an important role in the area of Spatial filtering 2D Images between different FPGA Implementation. In the last decade there are many research work purposed in the area of the area of Spatial Filtering 2D Images. In this review paper focus on the different the area of Spatial Filtering 2D Images and it's specification. Also discuss the different problems arise in the area of Spatial Filtering 2D Images such as Image Processing Applications, FPGA, 2-D filter. These are the major problems discuss in this survey paper.**

***Keywords*— Image Processing Applications, FPGA, 2-D filter, etc……**

I. INTRODUCTION

In the present era of modern world no field is devoid from the application of digital image processing. Starting from commercial fields to the field of health and security, image processing has a key role to play. Basically any image can be enhanced in two domains i.e. the spatial domain and the frequency domain to make it more applicable for a particular application. The spatial domain can again be classified into two major categories i.e. point operations and masking operations. Spatial domain masking operations, otherwise known as the filtering techniques operates directly on image plane, i.e. all the operations are performed on the pixels of the image. It works on neighbors of any particular pixel value. A spatial mask is chosen for this purpose of m mu size.

The mask is applied on any intensity value which is considered to be the centre pixel. During the operation size of the image must be same as the size of the window. Response of the filter is calculated by sum of product operation. After the operation is performed the mask is shifted to the next point. Fig.1 illustrates the spatial filtering operation considering a window size of 3 3u . It is performed on the 8-neighbors of the centre pixel. Again considering the number of pixels involved spatial filtering is further classified into two categories,

1) Linear filtering and
2) Non-linear filtering.

Linear filtering involves linear operation on pixels while non-linear filtering is based on the arrangement or ordering of the pixel values. One such example of spatial filtering is image smoothing. It is one of the steps of preprocessing of image before it goes for extraction of features or attributes. It involves removal of small details of the image, i.e. bridging of the gaps between lines or curves. Removal of small details signifies smoothing the abrupt transitions in the gray level of an image. Being low pass filtering operation it reduces the noise present at higher frequencies. It is helpful in object detection due to its ability to represent the overall object of interest without removing any useful information, which is achieved by harmonizing the intensity of less details with the background and the part having more information becomes more prominent. Image blurring deals with removing the noise spikes, i.e. pixels having exceptionally low or high values. Hence it is less helpful for the images corrupted by the Gaussian noise. A large spectrum of applications digital image processing has proved itself as an evergreen and ever growing field which makes the real time implementation even more compulsive. The advantages of FPGA like high speed and reconfigurable capabilities, helps in real time implementation of image processing algorithms. In our proposed work the emphasis has been given to reduce the time constrain and improving the speed so as to make the algorithms more suitable for real time applications. transformers.

II. LITERATURE SURVEY

Al-Dujaili, A., & Fahmy, S. A. (2017). This paper has compared two-dimensional image filter designs including transpose and direct form approaches. For direct form, different adder tree designs were compared. Considered use of the DSP blocks found in modern FPGAs results in an architecture that can achieve throughput close to the theoretical maximum for the architecture. Through detailed architecture-aware design, these filters can process a 640 × 480 video stream at over 1300 frames per second, or Full HD (1920 × 1080) video at over 190 frames per second while taking care of border pixels. The presented designs are released for use by the community and can be found at https://github.com/ash-aldujaili/spatial-filter-hdl.

Kumar, A., Rastogi, P., & Srivastava, P. (2015). HAAR DWT has been proved a novel process of text extraction considering multiple cases of image with its textual contents. The chip development and FPGA synthesis is a concept of segmenting the image into different regions to extract the textual information may be in horizontal, vertical, inclined. It also uses the methodology of sliding window for reading sub bands of high frequency. The simulation work is carried out for text regions are refined with the integration of mathematical operations such as dilation, erosion, closing and opening in the developed chip. The synthesis on Virtex-5 FPGA is carried out successfully and results are shown on host computer. The chip integration and methodology is very much successful to extract the textual information from a documentary image.

Saini, P., Kumar, A., & Singh, N. (2013). The design IC's for 2D and 3D image enhancement chip that leads the low power and optimized design is done in VHDL programming environment. In contrast the development is done to make programmable image chip to increase the efficiency, lower the power requirement, and reduce the delay with the comparison of previous work. Such chips can be used in digital cameras, digital oscilloscope etc. VHDL has been used to write all the programs for the IC's because of its userfriendly nature and thus modifications if required for further development shall not prove to be an obstacle. Thus the research focuses on simulation prior to fabrication. Burning these programs on FPGA (Field Programmable Gate Array) will help us to see the functional design of ICs. These results in addition to the systematic view generated would help us to design Application Specific ASIC. This work is a significant effort towards total digitization of image processing and would surely prove a boon for VLSI design industry.

Mehra, R., & Verma, R. (2012). The proposed design can work by using lesser number of look up tables to produce cost effective solution for edge detection system. Xilinx DSP tool simulation and testing when implemented on Virtex 2P FPGA can work at an estimated frequency of 148.133 MHz and shows an improvement of one fifth hardware utilization over the existing design. Future scope can be extended to achieve more improvement in terms of speed by using partial serial architecture.

Cho, Y. C. P., Bae, S., Jin, Y., Irick, K. M., & Narayanan, V. (2011, September). In this paper, we have presented design options for efficiently implementing the Gabor function for modeling V1 simple cells on FPGA with optimizations focused on minimizing resource usage to maximize performance by parallelizing more Gabor functions on FPGA. General 2D convolution on FPGA to apply the Gabor function is resource (DSP slice) demanding. The Gabor optimized convolution engine is shown to reduce DSP slice consumption by almost half compared to general 2D convolution. FPGA architectures for the steerable and rotated separable Gabor function method can further reduce DSP slice usage at the cost of accuracy of approximating Gabor functions. Section III gives a overall idea of the linear filtering and statistical windows used. The hardware design of the respective masks explained in Section IV. All the results based on the hardware requirement, speed of the design along with the desired outputs are shown in section V. Section VI gives the conclusion and explains the novelty of this approach.**[04]**

III. SPATIAL FILTERING

Spatial filtering techniques refer to those operations where the resulting value of a pixel at a given coordinate is a function of the original pixel value at that point as well as the original pixel value of some of its neighbors. These operations are classified into linear filtering operations and non-linear filtering operations.

In linear filters, the resulting output pixel is computed as a sum of products of the pixel values and mask coefficients in the pixel's neighborhood in the original image. In other words, if the function by which the new grey value is calculated is a linear function of all the grey values in the mask, then the filter is referred to as a linear filter. Mean filter is an example of linear filter.

In non-linear filters, the resulting output pixel is selected from an ordered sequence of pixel values in the pixel's neighborhood in the original image. Median filter is an example of non-linear filter.

As have been mentioned before in earlier lectures, some neighborhood operations work with the values of the image pixels in the neighborhood and the corresponding values of a sub image that has the same dimensions as the neighborhood.

The sub image is called a filter, mask, kernel, template, or window. The values in a filter sub image are referred to as coefficients rather than pixels.

These neighborhood operations consists of:

1. Defining a center point, (x,y)
2. Performing an operation that involves only the pixels in a predefined neighborhood about that center point.
3. Letting the result of that operation be the "response" of the process at that point.

4. Repeating the process for every point in the image.

The process of moving the center point creates new neighborhoods, one for each pixel in the input image. The two principal terms used to identify this operation are neighborhood processing or spatial filtering, with the second term being more common.

If the computations performed on the pixels of the neighborhoods are linear, the operation is called linear spatial filtering; otherwise it is called nonlinear spatial filtering.

Linear Spatial Filtering

For linear spatial filtering, the response is given by a sum of products of the filter coefficients and the corresponding image pixels in the area spanned by the filter mask. For the 3 X 3 mask shown in the previous figure, the result (response), R, of linear filtering with the filter mask at a point (x,y) in the image is:

$R = w(-1,-1)\, f(x-1, y-1) + w(-1,0)\, f(x-1, y) + \dots + w(0,0)\, f(0,0) + \dots + w(1,0)\, f(x+1, y) + w(1,1)\, f(x+1, y+1)$

which we see is the sum of products of the mask coefficients with the corresponding pixels directly under the mask.

Note in particular that the coefficient w(0,0) coincides with image value f(x,y), indicating that the mask is centered at (x,y) when the computation of the sum of products takes place. For a mask of size m X n, we assume that $m = 2a + 1$ and $n = 2b + 1$, where a and b are nonnegative integers. All this says is that out focus in the following discussion will be on masks of odd sizes, with the smallest meaningful size being 3 X 3, (we exclude from our discussion the trivial case of a 1 X 1 mask).

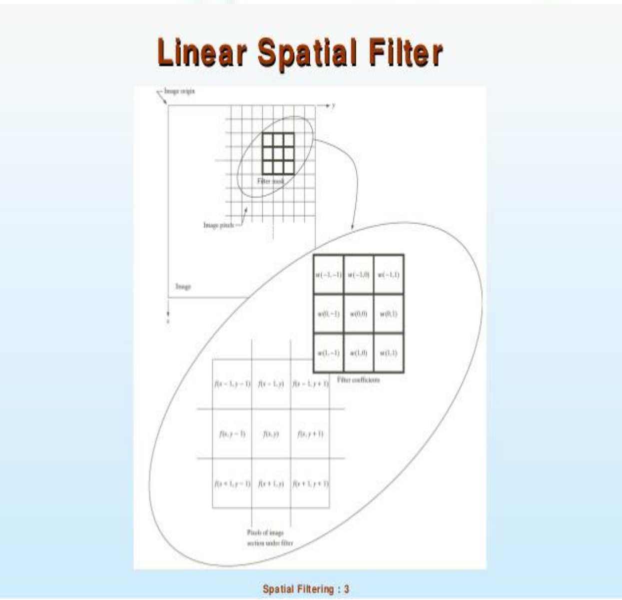

Fig 3.1 Linear Spatial Filtering

In general, linear filtering of an image f of size M X N with a filter mask of size m*n is given by the expression:

There are two closely related concepts that must be understood clearly when performing linear spatial filtering. One is correlation; the other is convolution.

Correlation is the process of passing the mask w by the image array f.

Mechanically, convolution is the same process, except that w is rotated by 180 degrees prior to passing it by f.

Nonlinear Spatial Filtering

Nonlinear Spatial Filtering is based on neighborhood operations also, and the mechanics of defining m X n neighborhoods by sliding the center point through an image are the same as discussed in the linear spatial filtering. However, whereas linear spatial filtering is based on computing the sum of products (which is a linear operation), nonlinear spatial filtering is based, as the name implies, on nonlinear operations involving the pixels of a neighborhood. For example, letting the response at each center point be equal to the maximum pixel value in its neighborhood is a nonlinear filtering operation. Another example, using log function.

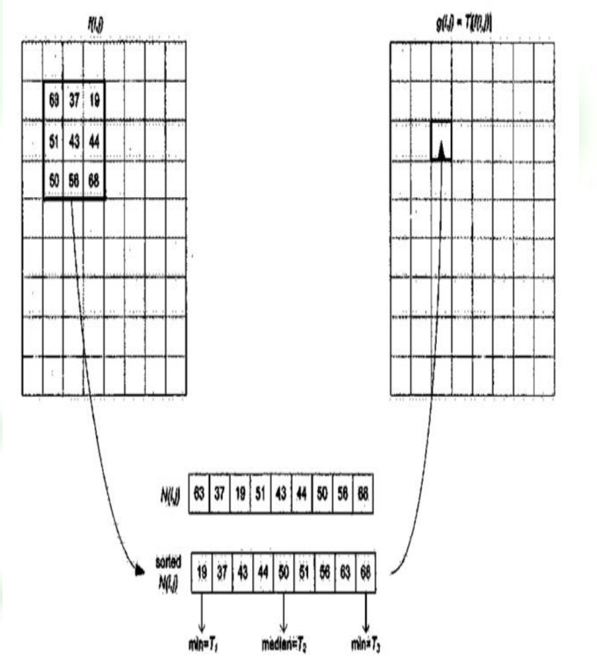

Fig 3.2 Nonlinear Spatial Filtering

IV. CONCLUSION AND FUTURE WORK

In this survey paper focus on A Literature Survey FPGA Implementation Of Spatial Filtering 2D Images. The important outcome of this paper is shown in the section of comparative analysis. In this survey paper observe that the mutual coupling is the major problem in A Literature Survey FPGA Implementation Of Spatial Filtering 2D Images. Also most of the design vision domains from lower gain problem. In future design a better A Literature Survey FPGA Implementation Of Spatial Filtering 2D Images. That can improve all these problem in this tracking and receiving the information, vision-based vehicle detection. In future try to fast Fourier. that can conform good better result in terms Spatial Filtering 2D Images.

REFRENCES

[1] Al-Dujaili, Abdullah, and Suhaib A. Fahmy. "High Throughput 2D Spatial Image Filters on FPGAs." *arXiv preprint arXiv:1710.05154* (2017).

[2] Kumar, Adesh, Prakshi Rastogi, and Pragyan Srivastava. "Design and FPGA implementation of DWT, image text extraction technique." *Procedia Computer Science* 57 (2015): 1015-1025.

[3] Saini, Priyanka, Adesh Kumar, and Neha Singh. "FPGA implementation of 2D and 3D image enhancement chip in HDL environment." *International Journal of Computer Applications* 62.21 (2013).

[4] Hanumantharaju, M. C., M. Ravishankar, and D. R. Rameshbabu. "Design and FPGA implementation of an 2D Gaussian surround function with reduced on-chip memory utilization." *2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI)*. IEEE, 2013.

[5] Gabiger-Rose, Anna, et al. "An FPGA-based fully synchronized design of a bilateral filter for real-time image denoising." *IEEE Transactions on Industrial Electronics* 61.8 (2013): 4093-4104.

[6] Mehra, Rajesh, and Rupinder Verma. "Area efficient fpga implementation of sobel edge detector for image processing applications." *International Journal of Computer Applications* 56.16 (2012).

[7] Christe, S. Allin, M. Vignesh, and A. Kandaswamy. "An efficient FPGA implementation of MRI image filtering and tumor characterization using Xilinx system generator." *arXiv preprint arXiv:1201.2542* (2012).

[8] Kaur, Sugreev, and Rajesh Mehra. "High Speed and Area Efficient 2D DWT Processor based Image Compression" Signal & Image Processing." *arXiv preprint arXiv:1101.0262* (2010).

[9] Cho, Yong Cheol Peter, et al. "Exploring Gabor filter implementations for visual cortex modeling on FPGA." *2011 21st International Conference on Field Programmable Logic and Applications*. IEEE, 2011.

[10] Yao, Lifan, et al. "An architecture of optimised SIFT feature detection for an FPGA implementation of an image matcher." *2009 International Conference on Field-Programmable Technology*. IEEE, 2009.

[11] Yao, Lifan, et al. "An architecture of optimised SIFT feature detection for an FPGA implementation of an image matcher." *2009 International Conference on Field-Programmable Technology*. IEEE, 2009.

[12] Díaz, J., et al. "Local image phase, energy and orientation extraction using FPGAs." *International Journal of Electronics* 95.7 (2008): 743-760.

[13] Abche, Antoine B., et al. "An FPGA implementation of a high resolution phase shift beamformer." *2007 IEEE International Conference on Signal Processing and Communications*. IEEE, 2007.

[14] Torres-Huitzil, César, and Miguel Arias-Estrada. "FPGA-based configurable systolic architecture for window-based image processing." *EURASIP Journal on Applied Signal Processing* 2005 (2005): 1024-1034.

[15] Muthukumar, Venkatesan, and Daggu Venkateshwar Rao. "Image processing algorithms on reconfigurable architecture using HandelC." *Euromicro Symposium on Digital System Design, 2004. DSD 2004.*. IEEE, 2004.

