A Novel Cascaded Multilevel Inverter Using Mcpwm With Minimum Switches

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***Abstract*— Multilevel inverter presents attractive advantages in high power applications. The proposed method is 15- level multilevel inverter which has number of modules in series. Each module has one switch and one parallel connected diode. The proposed method involves less number of switches with more number of voltage levels. In this paper, MCPWM technique is proposed to reduce the THD value less than 2% and increases the efficiency. It drastically reduces the switches for high number of levels and improves the total harmonic distortion (THD).**

***Keywords*— cascaded multilevel inverter, H-bridge inverter, Total Harmonics Distortion, Multicarrier pulse width modulation.**

I. INTRODUCTION

Nowadays industrial applications require high power apparatus in recent years. The utility applications require medium voltage and MW power level. For an intermediate voltage grid, it is troublesome to connect single power semiconductor switch directly [1]-[2]. The utilization of ac changing frequency speed regulations is widely popularized. High power and medium voltage inverter has currently become a research target but there are many problems associated with conventional two level inverter.

Multilevel inverter have been achieved more concentration for high power application in recent years which can operate at high switching frequencies while generating lower order harmonic components [3]-[4].

A multilevel inverter not only achieves large power ratings, but also allows the use of renewable energy sources. There are several topologies such as neutral point clamped or diode clamped multilevel inverter, flying capacitor based multilevel inverter, cascaded H-bridge multilevel inverter and hybrid H-bridge multilevel inverter. The main disadvantage of diode clamped multilevel inverter topology is restriction to the high power operation.

The basic topology introduced is the series H-bridge design [5]-[6], in which several configurations have been obtained. This topology made of series power conversion cells which form the cascaded H- bridge multilevel inverter and power levels may be scaled easily.

An apparent fault of this topology is the requirement of large number of isolated voltage sources. The proposed topology for cascaded multilevel inverter has high number of steps associated with low number of power switches. In addition, for generating the levels at the output voltage, a procedure for manipulative the required dc voltage source is proposed.

II. HYBRID MULTILEVEL INVERTER

The accepted structure of the hybrid multilevel inverter for single phase is shown in figure.1. Each H-bridge circuit is connected in series associated with it. Each of the circuit consists of four active switching elements that can make the output voltage as positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit.

A common multilevel inverter topology employs multiple/link voltage of equal magnitudes. It is kind of easy to generalize the number of distinct levels [7] - [8].

The A may be number of stages or dc sources and the associated number output level can be written as follows

$$N \text{ level} = 2A+1 \qquad (1)$$

The topology is used number of switches in this equation is expressed as,

$$N \text{ switch}=4\ A \qquad (2)$$

The benefit of the hybrid multilevel inverter is modularized structure. This will enable the manufacturing process to be done faster and economically.

The fault of this topology needs a separate dc source for each of the H-bridges and involves high number of semiconductor switches.

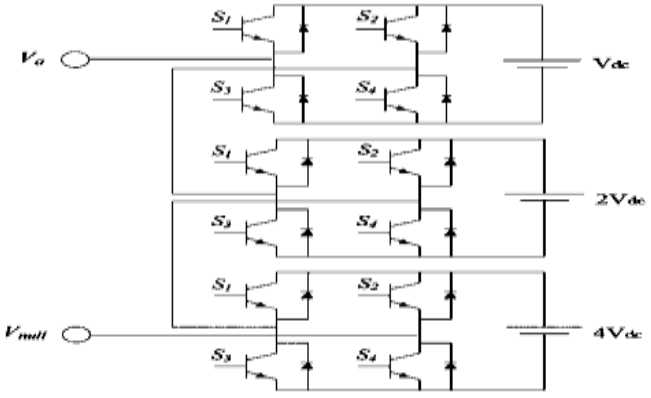

Figure.1 Topology for Hybrid Multilevel Inverter

III. PROPOSED METHOD

A. Cascaded Multilevel Inverter

The proposed cascaded multilevel inverter has a general structure of the cascade multilevel inverter is shown in figure. 2. The each separate voltage sources (1Vs, 2Vs, 4Vs) is connected in series with other sources via a special circuit associated with it. The each stage of the circuit consists of only one active switching element and one bypass diode that diode makes the multilevel output voltage as positive one with several levels.

The basic operation of modified cascaded multilevel inverter for producing the output voltage as +1Vdc is to turn on the switch S1 (S2 and S3 turn off) and turn on S2(S1 and S3 turn off) for producing output voltage as +2Vdc. Similarly other levels can be achieved by turn on the suitable switches at particular intervals; Table.1 shows the basic operation of proposed cascaded multilevel inverter. From the table it can be inferred that only one H-bridge is connected to get both positive and negative polarities.

The main advantage of cascaded H-bridge multilevel inverter is high number of levels with reduced number of switches.

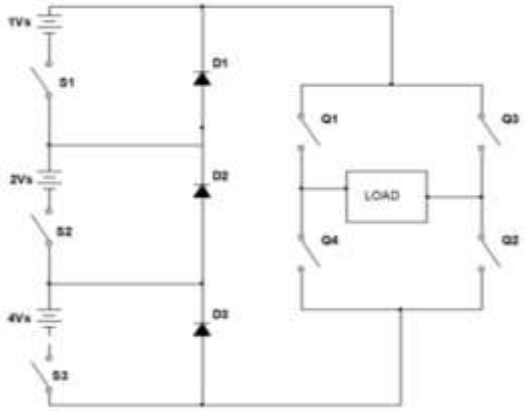

Figure.2 Topology for Cascade Multilevel Inverter

The A number of dc sources or stages and the associated number output level can be calculated by using the equation

$$N\ level = 2A+1-1 \quad (3)$$

Voltage can be calculated on each stage by using the equation

$$V = 2A-1.Vdc \quad (4)$$

The topology is used number of switches in this is given by the equation

$$N\ switch = A + 4 \quad (5)$$

Table 1: Basic Operation of Modified Hybrid Multilevel Inverter

S.NO	Intervals	On switches	Off switches	Voltage levels	Current flow path
1	I	S1	S2,S3	+1Vs	S1,D2,D3
2	II	S2	S1,S3	+2Vs	S2,D1,D3
3	III	S1,S2	S3	+3Vs	S1,S2,D3
4	IV	S3	S1,S2	+4Vs	D1,D2,D3
5	V	S1,S3	S2	+5Vs	S1,D2,D3
6	VI	S2,S3	S1	+6Vs	D1,S2,S3
7	VII	SI,S2,S3	-	+7Vs	S1,S2,S3
8	VIII	-	S1,S2,S3	0	D1,D2,D3

The figure. 3 shows the typical output voltage waveform of a 15-level cascaded multilevel inverter with 3 separate dc sources.

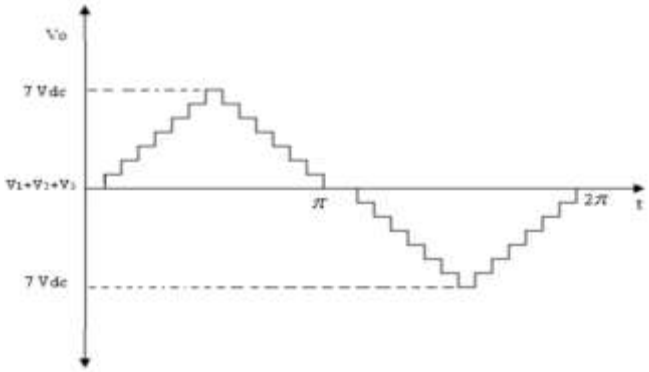

Figure .3 Typical output waveform for Cascaded Multilevel Inverter

B. Total Harmonic Distortion (THD)

The Total Harmonic Distortion block measures the Total Harmonic Distortion (THD) of a periodic signal. The signal can be voltage or current. The THD is defined as the ratio of Root Mean Square (RMS) value of the total harmonics of the signal to the RMS value of its fundamental signal. The THD value will be zero for a pure sinusoidal voltage or current. For example, for currents, the THD is defined as

$$\text{Total Harmonic Distortion (THD)} = I_h / I_n$$

Where ($I_h = I_{22} + I_{32} + \ldots + I_{n2}$), I_n=RMS value of the harmonic 'n', I_f= RMS value of the fundamental current.

IV. SIMULATION MODELS

A. Simulation model of Proposed System

The simulation model of proposed system is shown in the Figure 4. The 15-level cascaded multilevel inverter has been developed using MATLAB. The proposed method is used to get sinusoidal waveform and reduced harmonics with minimum number of components. Therefore the efficiency of the cascaded multilevel inverter is increased. The low order harmonics are reduced. This model is used to produce the unidirectional output in both positive and negative directions.

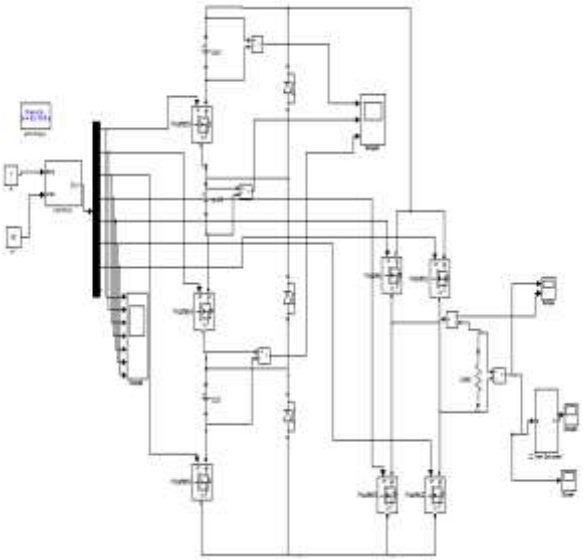

Figure .4 Simulation Diagram of Proposed System

B. Results and Discussion

The simulation results and analysis of 15-level cascaded multilevel inverter with reduced number of switches is shown below. It describes the output voltage waveform and output current waveform with R load.

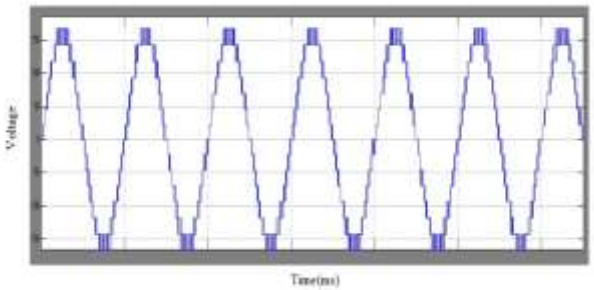

Figure 5. Output Voltage Waveform of cascaded MLI for R-load

The multilevel output voltage for CMLI with R load is shown in the Figure 5. It has 15 levels. The cascaded multilevel inverter output waveform has different levels of voltage like 24V, 48V, 96V in both polarities. It can be achieved by selection of switching pattern. The fundamental frequency of CMLI is 50Hz.

The output current for the R load is shown in the Figure 6. It has drawn between the time and current.

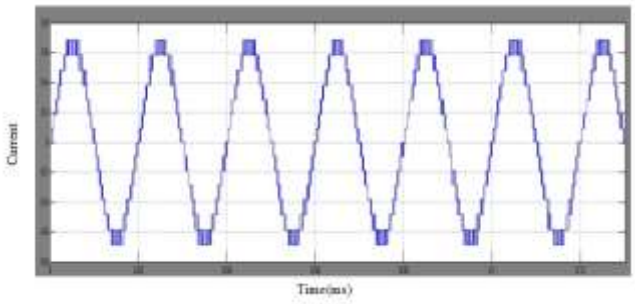

Figure 6. Output Current Waveform of cascaded MLI with R-load

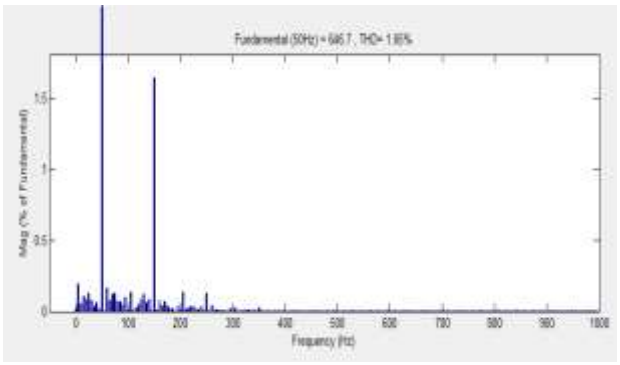

Figure .7 Spectrum Analysis of Total Harmonic Distortion for CMLI with R-load

The modified hybrid multilevel inverter FFT analysis is shown in the Figure.7 for R load. Analysis of THD (Total Harmonic Distortion) plays a major role in case of inverters.

Table 2: Justification of the System

S.No	Contents	Existing system	Proposed system
1	Level of Inverter	9 level	15 Level
2	Technique	SOP	MCPWM
3	THD level	3.65	1.65
4	Efficiency	97%	98%

Cascaded multilevel inverters with many dc sources while minimizing several harmonics. In this cascaded multilevel inverter due to their high efficiency, low switching losses, and low electromagnetic interference. Overall, MCPWM is a good fitness evaluation to cascaded multilevel inverter, for flow measurement and control applications. Justification of the system shown in Table 2. From all the above discussions we can conclude that MCPWM has better harmonic minimization and fast response.

V. CONCLUSION

Cascaded multilevel inverter using MCPWM is proposed. The proposed system achieves high output voltage and reduced number of switches. MCPWM technique used here increase

the efficiency and decreases the harmonics. Cascaded multilevel inverter along with MCPWM makes the system is healthier. The system of fifteen level cascaded multilevel inverter can be further improved to real time application and pursuit of software will extend to hardware.

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