Induction Motor Fed L-Z Source Inverter Using Closed Loop Controller for Variable Speed Drives

Deepa.N#1, Jamuna.P#2
1 Department of Electrical Engg, Nandha Engineering College,
Anna university, India
1gokilamani07@gmail.com
2Head Of the Department, Department Of Electrical Engg, Nandha Engineering College,
Erode 638052,
Anna university, India

***Abstract*—This paper presents LZSI which only contains inductors and diodes in Z-source network with closed loop controller. The inverter uses a unique inductor and diode network for boosting its output voltage, provides a common ground for the dc source and inverter, especially in prohibiting the inrush current at start up and the resonance of Z-source capacitors and inductors. The inverter can increase the boost factor through adjusting shoot-through duty ratio and increasing the number of inductor. The working principle of the proposed L ZSI is analysed in detail. The closed loop speed controller is used to sense the speed and checks the error speed. It is used in variable speed drives .Simulation and experimental results are given to demonstrate the operation features of the inverter.**

***Index Terms*—Inductor, inrush current, power converters, resonance.**

I.INTRODUCTION

IN recent years, various Z-source inverter (ZSI) topologies have been presented in numerous diversified studies. Some of the studies are focused on applications, modelling, controls, and modulation strategies whereas others are focused on the development of new topologies. The ZSIs accomplish a single-stage power conversion with buck-boost capabilities. In ZSIs, both of the power switches in a leg can be turned on at the same time and thereby eliminate the dead time. This significantly improves the reliability and reduces the output waveform distortion. Fig. 1(a) shows the classical ZSI in which the two-port impedance network couples the main inverter circuit to the dc source. In order to overcome the shortcomings of the classical ZSI, the quasi-ZSI (qZSI) shown in Fig. 1(b) and SL-ZSI shown in Fig. 1(c) were developed.

Despite the aforementioned merits, the aforementioned ZSI topologies also show the following drawbacks:

1) Capacitors are used in the Z-source network, thus high-voltage or large capacity capacitors should be used, which may result in large volume, cost expensive, and reducing the life span of system;

2)It cannot suppress the inrush current and the resonance introduced by Z-source capacitors and inductors at start up, thus causing the voltage and current surge, which may destroy the devices;

3) It regulates boost factor only by adjusting the Shoot-through duty ratio.

To solve the aforesaid drawbacks in aforementioned ZSI, a new ZSI topology is presented with no capacitor and reducing inherent inrush current limitation at start-up. It can suppress the resonance thoroughly by removing capacitor and improve the efficiency of power supply. Also, no error is produced in the output by using closed loop speed controller. It senses the speed and also vary by v/f control.

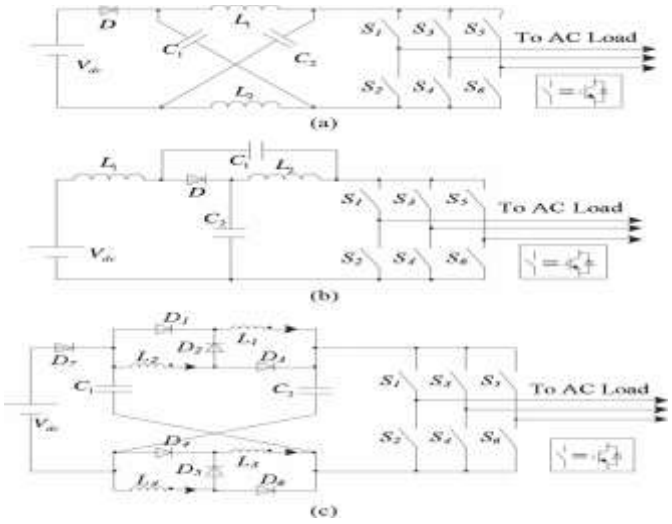

Fig. 1Impedance-network inverter topologies. (a) The classical ZSI, (b) quasi-ZSI, and (c) SL-ZSI.

II. L-Z-SOURCE INVERTER

Different to the original ZSI, the proposed inverter has no capacitor, and is composed of two inductors ($L1$, $L2$, and $L1 = L2$), and three diodes ($D1$,$D2$, and$D3$), as shown in Fig. 2. The combination of $L2 - L3 - D1 - D2 - D3$ acts as a switched inductor cell. The proposed topology provides inrush current suppression, unlike the traditional topologies,

because no current flows to the main circuit at start up. The proposed topology also provides a common ground for the source and inverter.

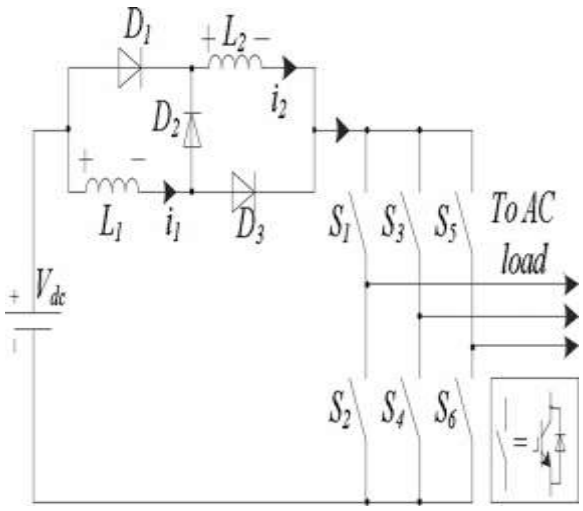

Fig. 2. L-ZSI with two inductors.

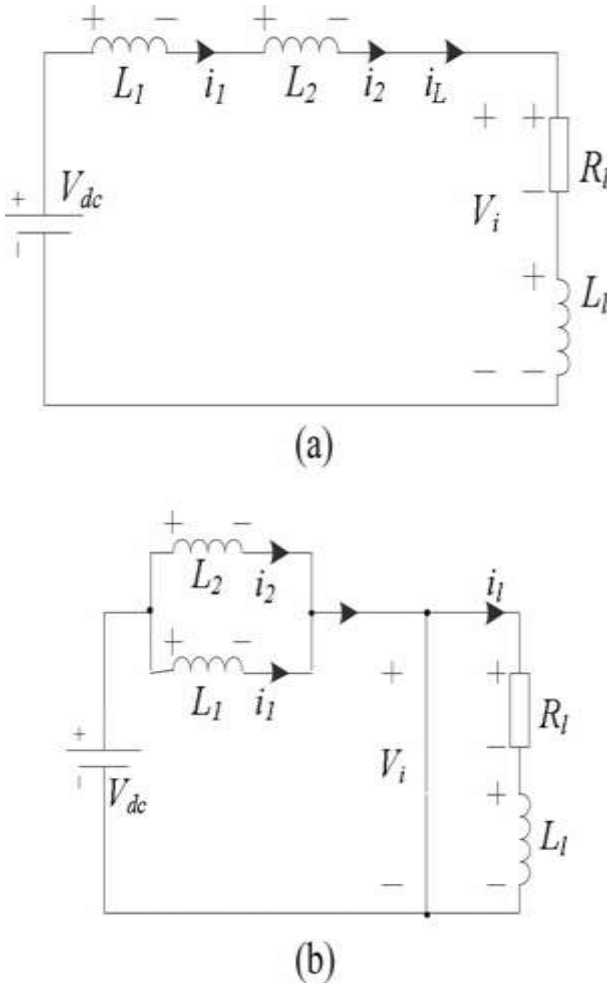

Fig. 3. Operating states: (a) non-shoot-through and (b) shoot-through state.

A. Operation Principles

Unlike the traditional ZSIs, L-ZSI just has shoot-through zero states besides the traditional six active states. The operating principles of the proposed inverter are also similar to those of the classical ZSI. For the purpose of analysis, the operating states are simplified into shoot-through and non-shoot-through states. Fig. 3 shows the equivalent circuits of L-ZSI. In the non-shoot-through state, as shown in Fig. 2, *D*2 is on, while *D*1 and *D*3 are off. *L*1 and *L*2 (*L*1 = *L*2 = *L*) are connected in series. *L*1 and *L*2 transfer energy from the dc voltage source to the main circuit, and the equivalent circuit is shown in Fig. 3(a). The corresponding voltages across *L*1 and *L*2 in this state are *V*1 non and *V*2 non, respectively. Thereby, (1) and (2) can be contained

$$V1\ \text{non} + V2\ \text{non} + Vi = V\text{dc} \quad (1)$$

$$V1\ \text{non} = V2\ \text{non}. \quad (2)$$

From (1) and (2), (3) and (4) can be concluded

$$V1\ \text{non} = 1/2V\text{dc} - 1/2Vi \quad (3)$$

$$V2\ \text{non} = 1/2V\text{dc} - 1/2Vi \quad (4)$$

where *V*dc is the dc source and *Vi* is the dc-link voltage.

In the shoot-through state, as shown in Fig. 2, the inverter side is shorted by both the upper and lower switching devices of any phase leg. During the shoot-through state, *D*2 is off, while *D*1 and *D*3 are on. *L*1 and *L*2 are connected in parallel, and inductors *L*1 and *L*2 store energy. The equivalent circuit is shown in Fig. 3(b). The corresponding voltages across *L*1 and *L*2 in this state are *V*1 and *V*2 , respectively, and (5) is obtained

$$V1 = V2 = V\text{dc}. \quad (5)$$

$$Il = (1 + D)/\ V\text{dc}\ Rl \quad (6)$$

where *B* is the boost factor; *IL* is the inductor current; *Il* is the load current; *D* is shoot-through duty cycle.

B. Extension of the Z-Source Impedance Network

Through the earlier analysis, it can be known that switched inductor cell can improve the voltage gain. Based on this feature, the Z-source network can be extended as shown in Fig. 4.The operating principle is analyzed as follows. In the non-shoot-through state, as shown in Fig. 4, *D*1,2 ,*D*2,2, . . . , *Dn*−1,2 , and *Dn*,2 are on, while *D*1,1,*D*1,3,*D*2,1 ,*D*2,3, . . . , *Dn*−1,1,*Dn*−1,3,*Dn*,1 , and *Dn*,3 are off. *L*1, *L*2 , . . .,*Ln*−1 , and *Ln* are connected in series. *L*1, *L*2 , . . ., *Ln*−1 , and *Ln.*

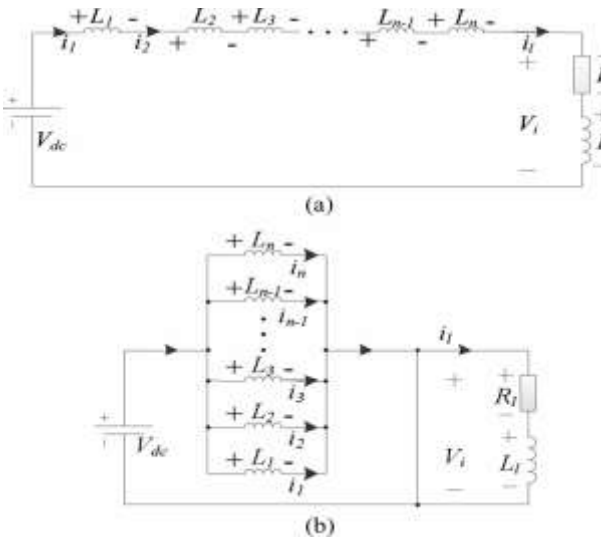

Fig. 5. Operating states: (a) non-shoot-through and (b) shoot-through state.

transfer energy from the dc voltage source to the main circuit, and the equivalent circuit is shown in Fig. 5(a). The corresponding voltages across *L*1, *L*2 , . . ., *Ln*−1 , and *Ln* in this state are *V*1 non, *V*2 non, *V*3 non, . . ., *Vn*−1 non, and *Vn* non, respectively.
Thus, (11) and (12) can be contained

$$V1\ \text{non} + V2\ \text{non} + \cdots + Vn-1\ \text{non} + Vn\ \text{non} + Vi = V\text{dc} \quad (7)$$

$$V1\ \text{non} = V2\ \text{non} = \cdots = Vn-1\ \text{non} = Vn\ \text{non}. \quad (8)$$

In the shoot-through state, as shown in Fig. 4, the inverter side is shorted by both the upper and lower switching devices of any phase leg. During the shoot through state, *D*1,2,*D*2,2, . . . , *Dn*−1,2 and *Dn*,2 are off, while *D*1,1,*D*1,3,*D*2,1,*D*2,3, . . . , *Dn*−1,1,*Dn*−1,3,*Dn*,1 and*Dn*,3 are on. *L*1, *L*2 , . . ., *Ln*−1 and *Ln* are connected in parallel, inductors *L*1, *L*2, . . . , *Ln*−1 and *Ln* store energy, and the equivalent circuit is shown in Fig. 5(b). (13) is obtained.

$$V1 = V2 = \cdots = Vn-1 = Vn = V\text{dc} \quad (9)$$

Applying the volt-second balance principle to each inductor,

$$B = 1 + (n - 1)D/1 - D \quad (10)$$

$$IL = I1 = I2 = \cdots = In-1 = In = nL+Ll)+L(1-D)/RlL(1 - D)\ V\text{dc} \quad (11)$$

The boost factor of L-ZSI is increased with the increasing number of inductors, and the number of inductors is not limited. The range of *D* is [0, 1).

III. FEATURES COMPARISON WITH OTHER ZSI TOPOLOGIES

A. Boost Ability and Stress Comparison

Different control and load conditions provide varied stresses of impedance-type power inverters. For comparison, the proposed L-ZSI, SL-ZSI, and the classical ZSI are simplified. The ac-side circuit is represented by its simplified equivalent dc load [20]. A resistive load impedance (*Rl*) connects directly in parallel with active switch *S*, where *il* and *vl* are the instantaneous load current and voltage. Using the steady-state analysis method and the maximum boost control method. we obtain the voltage and current stresses on the main components, such as *L* and *C*. Table I compares the governing equations of the proposed L-ZSI, SL-ZSI, and the classical ZSI with the same *D* and *V*dc. Compared with the classical ZSI and SL-ZSI, the proposed inverter can increase the voltage boost inversion ability through adjusting short shoot-through duty ratio or the number of inductor as shown in Fig. 6. From Fig.67, it can be seen that voltage gain is increased with the increasing of shoot-through duty ratio and the increasing of the number of inductors.

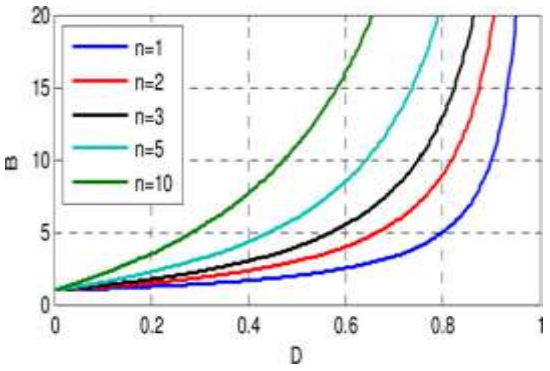

Fig. 6. Boost factor of L-ZSI under different number of inductor.

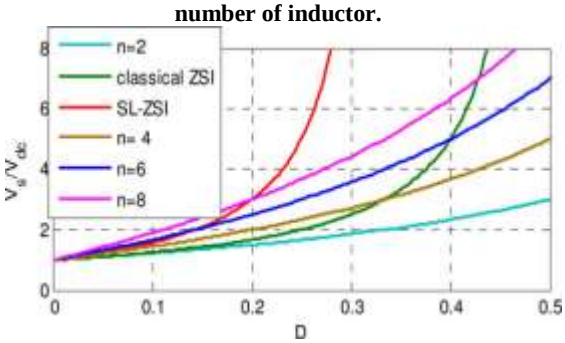

Fig. 7. Switching device voltage stress for classical ZSI, SL-ZSI, and L-ZSI.

Fig. 7 shows the switching device voltage stress curves. So the voltage stress *Vs* is the same in classical ZSI, SL-ZSI, and L-ZSI with same boost factor.

B. Inrush Current and Voltage Overshoot Analysis

In L-Z-source impedance network, there is no capacitor as shown in Fig. 4. The proposed topology provides inrush current suppression, and no current flows to the main circuit at start-up. So there is no voltage overshoot phenomenon causing by capacitor, and this topology can improve the transition process.

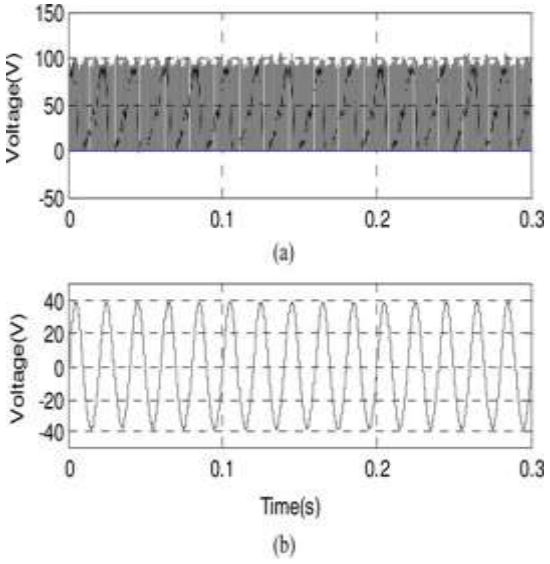

Fig. 8. Simulation results for L-ZSI under n = 4, M = 0.8 and D = 0.2.(a) DC link voltage. (b) Output phase voltage.

III.PROPOSED SYSEM

A.BLOCK DIAGRAM

In Existing system, there is no feedback loop. It is a open loop control system and the speed is varied nearly rated speed.To overcome this problem,closed loop speed controller is used.Here,PIC controller is used to sense the speed.so,the speed is varied by v/f control.It is used in variable speed drives such as rated,below rated and above rated speed based on the industrial applications.

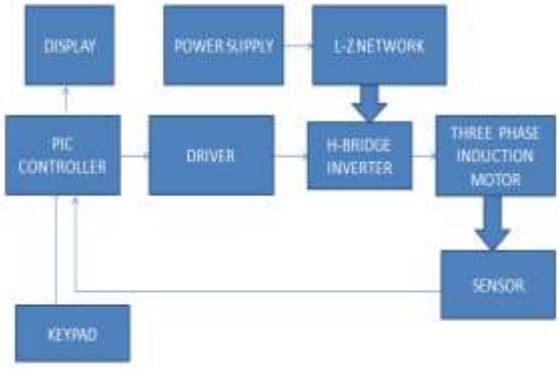

Fig.9.Block diagram of proposed system

The supply is given to the impedance network. The output voltage is fed to the H-bridge inverter and it produces the ac voltage .It is used for v/f control for variable drives and the ac voltage from the inverter is fed to the single phase induction motor. It starts to rotate and the speed is sensed by the PI controller. At first, the values are set in keypad based on the application. The PIC controller has A/D unit to sense the signals and displays in the display unit. The driver is used for controlling and high power applications.

B.PIC CONTROLLER

Fig.10.PIN DIAGRAM OF PIC 16F887

PICs are popular with developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and re-programming with flash memory) capability.

The RA,RB RC and RD are the general purpose registers. It has 40 bits. The pin 17 is used to run the motor.PWM is used.ADC is inbuilt in PIC controller. The port 33 is an external interrupt .This port is directly connected to keypad to reset the values.

The PIC architecture is distinctively minimalist. It is characterized by the following features:

1) Separate code and data spaces (Harvard architecture).
2) A small number of fixed length instructions.
3) Most instructions are single cycle execution (4 clock cycles), with single delay cycles upon branches and skips
4) A single accumulator (W), the use of which (as source operand) is implied. All RAM locations function as registers as both source and/or destination of math and other functions.
5) The PWM port is used to produce the pulse signal to operate the controller.
6) PICs have a set of registers that function as general purpose RAM. Special purpose control registers for on-chip hardware resources are also mapped into the data space.
7) The addressability of memory varies depending on device series, and all PIC devices have some banking mechanism to extend the addressing to additional memory.

IV.SIMULATION RESULTS

The simulation model of L Z-source inverter is shown in the Figure 6.1 The L Z-source inverter has been developed using MATLAB. The proposed method is used to vary the speed and improve the performance of the system. Therefore the efficiency of the LZ-source inverter is increased.

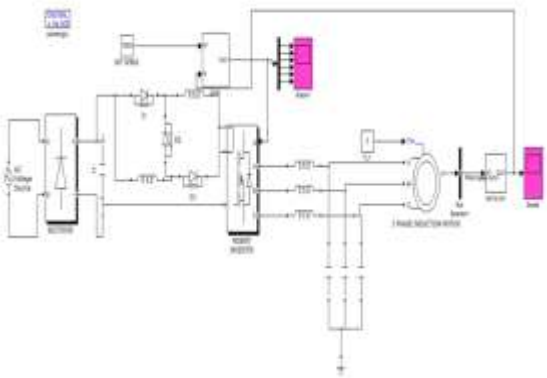

Fig.11simulation of induction motor fed L Z-Source inverter

The output waveform of the speed is shown in Fig.13.It shows the motor runs at variable speed. The fig.13 shows the waveform of the speed by V/F control method. The frequency is directly proportional to the speed. so, the actual speed and set speed is compared in the PID controller and the switch is ON based on the signal.

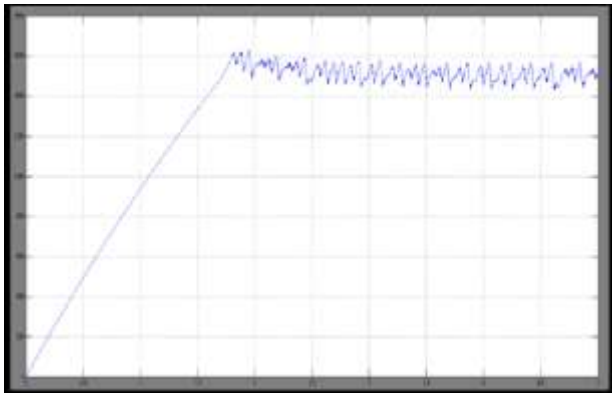

Fig.12. Simulation result of output speed using Closed Loop controller

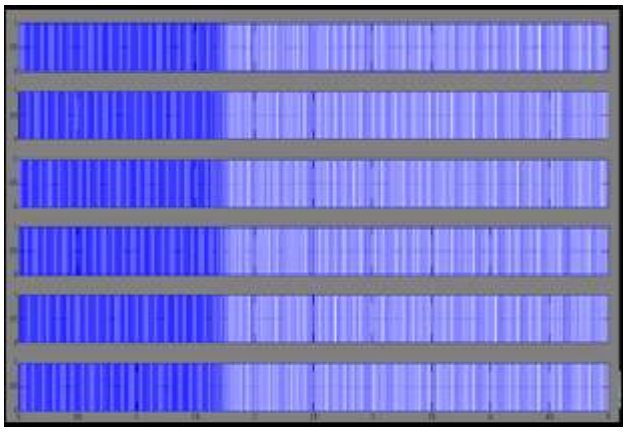

Fig. 13.Simulation Results of the v/f waveform

V. CONCLUSION

This paper has presented a L-ZSI by improving the performance with closed loop speed controller. The proposed inverter employs a unique inductor and diode network to couple the low dc voltage energy source to the main circuit of the inverter, and avoids the disadvantage causing by capacitor in the ZSI, especially in prohibiting the inrush current at start-up and the resonance of Z-source capacitors and inductors. The inverter can increase the voltage gain through adjusting shoot-through duty ratio and increasing the number of inductor.

The closed loop controller senses the signal and compare with reference signal and produces the speed value based on the industrial applications. Both the simulation and experimental results demonstrate its advantages. Therefore, the proposed inverter could be widely used in the variable speed drives based on the applications.

REFERENCES

[1] G. N. Veda Prakash and M. K. Kazimierczuk, "Small-signal modelling of open-loop PWM Z-source converter by circuit-averaging technique," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1286–1296, Mar. 2013.

[2] F. B. Effah, P.Wheeler, J. Clare, and A.Watson, "Space-vector-modulated three-level inverters with a single Z-source network," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2806–2815, Jun. 2013.
[3] F. Guo, L. Fu, C.-H. Lin, C. Li,W. Choi, and J.Wang, "Development of an 85-kW bidirectional quasi-Z-source inverter with DC-link feed-forward compensation for electric vehicle applications," *IEEE Trans. Power Electron.*,vol. 28, no. 12, pp. 5477–5488, Dec. 2013.
[4] K. Park, K.-B. Lee, and F. Blaabjerg, "Improving output performance of a Z-source sparse matrix converter under unbalanced input-voltage conditions," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 2043–2054,Apr. 2012.
[5] X. Liu, P. C. Loh, P. Wang, and X. Han, "Improved modulation schemes for indirect Z-source matrix converter with sinusoidal input and output waveforms," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4039–4050,Sep. 2012.
[6] O. Ellabban, J. Van Mierlo, and P. Lataire, "A DSP-based dual-loop peak DC-link voltage control strategy of the Z-source inverter," *IEEE Trans.Power Electron.*, vol. 27, no. 9, pp. 4088–4097, Sep. 2012.
[7] Y. Zhou, L. Liu, and H. Li, "A high-performance photovoltaic module integrated converter (MIC) based on cascaded quasi-Z-source inverters (qZSI) using eGaN FETs," *IEEE Trans. Power Electron.*, vol. 28, no. 6,pp. 2727–2738, Jun. 2013.
[8] P. C. Loh, F. Gao, P.-C. Tan, and F. Blaabjerg, "Three-level ac–dc–ac Z source converter using reduced passive component count," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1671–1681, Jul. 2009.
[9] Y. Tang, S. Xie, C. Zhang, and Z. Xu, "Improved Z-source inverter with reduced capacitor voltage stress and soft-start capability," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 409–415, Feb. 2009.
[10] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2,pp. 504–510, Apr. 2003.

