# Implementation of 6T SRAM Using NWL Technique

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***Abstract*— Memory arrays are an essential building block in any digital system. As the size of embedded system is shrinking with reduction in operating voltage, it has led to increased design challenge for the embedded engineer to meet the optimal demand of low power design of SRAM memory system. The aspects of designing an SRAM are very vital to designing other digital circuits as well. The majority of space taken in an integrated circuit is the memory. SRAM design consists of key considerations, such as increased speed and reduced layout area and also power dissipation is major issue and plays an important role in CMOS SRAM design due to increased integration. Semiconductor memory arrays are capable of storing large quantities of digital information which are essential to all digital systems. The ever increasing demand for larger data storage capacity has driven memory development towards more compact design and consequently toward higher storage densities. In this paper we have implemented SRAM using 0.12 µm using CMOS technique. The complete implementation and verification is done on the Tanner tool, Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit. The circuit is characterized by using the 0.12µm technology which is having supply voltage 0f 1.2volt.**

***Keywords*— CMOS SRAM, NLPP, PLNP, PMOSFET, NMOSFET, TANNER TOOL S-edit, L-edit, W-edit**

## Introduction

Static RAM plays a key role in modern devices as the technology advances and the need for high speed applications in very deep sub micron technology. SRAM stands for static random access memory which means that memory in which the data can be accessed in random order and since these RAMs can hold their stored data infinitely, provided the power supply remains on without refreshing since it uses latches as storage cells therefore these are called static RAMs. It is the volatile memory i.e. disconnection of the power supply results in a loss of the stored data. Static random-access memory continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high-end workstation and microprocessor applications. For almost all fields of applications, semiconductor memory has been a key enabling technology. It is forecasted that embedded memory in SOC designs will cover up to 90% of the total chip area. A representative example is the use of cache memory in microprocessors. The operational speed could be significantly improved by the application of on-chip cache memory that temporarily stored a fraction of the data and instruction content of the main memory. The power dissipation majors an important role in CMOS SRAM design due to increased integration. Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital systems. The ever increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently toward higher storage densities.

## Memory Organization

When implementing an N-word memory where each word is M bits wide. The most intuitiveapproach is shown in figure 2a. If we assume that this module is a single port memory. In other words, only one signal Si can be high at any time. Assume that we would like to implement a memory that holds 1 million (N=106) 8 bit (M=8) words. Since memory dimensions always come in powers of 2. In this particular case, the actual no. of words equals

$$2^{20} = 1024 \times 1024 = 1,048,576.$$

When implementing this structure using the strategy of figure 1a. We quickly realize that1 million select signals are needed. Since these signals are normally provided from off chip or from another part of the chip. This translates into a lot of wiring problems. A decoder is inserted to reduce the no. of select signals as shown in figure 2.b[11]. A memory word is selected by provided a binary encoded address word (A0 to Ak-1), the decoder translated this address into N=2k select lines, only one of which is active at a time. This virtually eliminates the wiring and packaging problems.

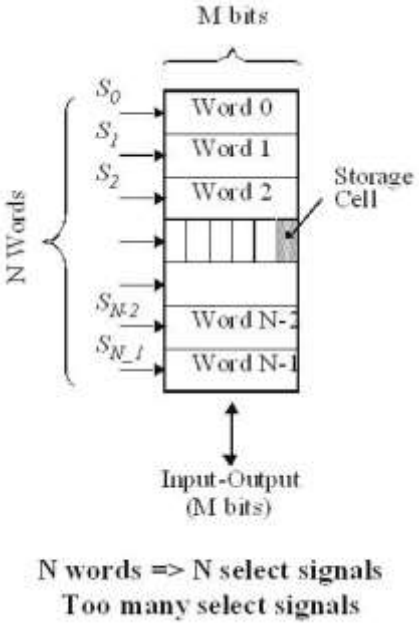
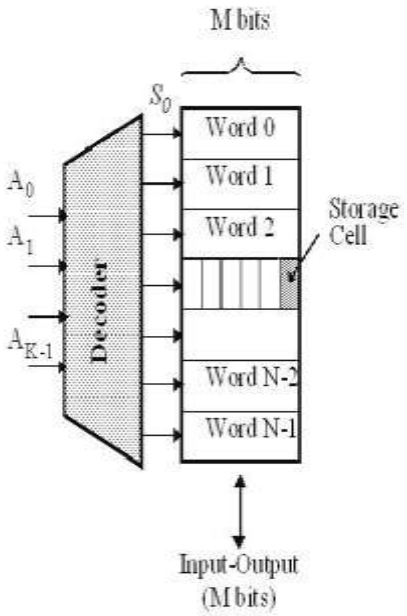



**Figure1**




Decoder reduces # of select signals

$K = log_2 N$

**Figure 2**

**SRAM 6T (SIX TRANSISTOR) CELL**

A six-transistor (6T) CMOS SRAM cell is as shown in figure 3a.It is similarly to one of the implementations of an SR latch, it consists of six transistors. Similarly to one of the implementations of an SR latch . it consists of six transistors. Four transistors $M_1$,$M_2$,$M_3$,$M_4$ comprise cross-coupled CMOS inverters and two transistors $M_5$ , $M_6$ are said to be a access transistors as it provide read and write access to the cell. the access transistors connect the two internal nodes of the cell to the true (BL) and the complementary ($\overline{BL}$) bit lines. Figure 3b shows a Tanner tool vesion of 6T SRAM cell

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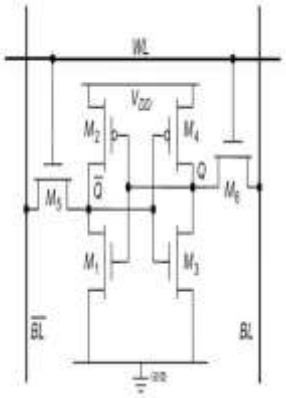


**Figure 3**

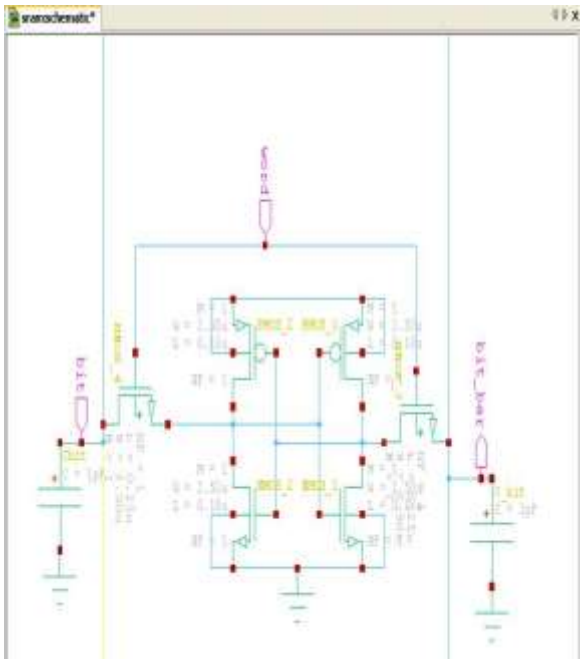

**Figure 4**

***A. Read Operation***

Before initiating a read operation, the bit lines are precharged to *VDD*. The read operation is initiated by enabling the word line (WL) and connecting the precharged bit lines, BL and $\overline{BL}$, to the internal nodes of the cell. Figure 3.1 shows the operation of various transistors. Consider the $\overline{BL}$ to side of the cell. The bit line capacitance for larger memories is in the pF range. Consequently, the value of $\overline{BL}$ stays at the precharged value VDD upon enabling of the read operation (WL→1). This series combination of two NMOS transistors pulls down the $\overline{BL}$ towards ground. As the difference between BL and $\overline{BL}$ builds up, the sense amplifier is activate to accelerate the reading process.

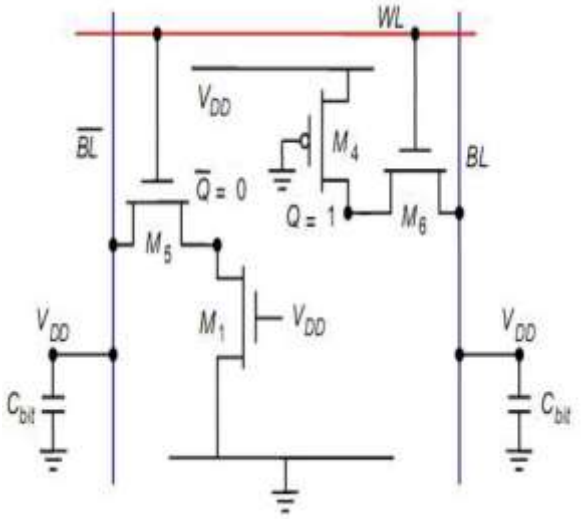


**Figure 5**

 

### *B. Write Operation*

Assume that a 1 is stored in the cell. A 0 is written in the cell by setting $\overline{BL}$ to 1 and BL to 0, which is identical to applying a reset pulse to an SR latch. This causes the flip-flop to change the state if the devices are sized properly. During the initiation of a write, the schematic of the SRAM cell can be simplified to the model of Figure 3.2 . It is reasonable to assume that the gates of transistors M1 and M4 stay at VDD and GND respectively, as long as the switching has not commenced. If transistors M4 and $M_6$ are properly sized, then the cell is flipped and its data is effectively overwritten. A statistical measure of SRAM cell write ability is defined as *write margin*. Write margin is defined as the minimum bit line voltage required to flip the state of an SRAM cell [12]. The write margin value and variation is a function of the cell design, SRAM array size and process variation.

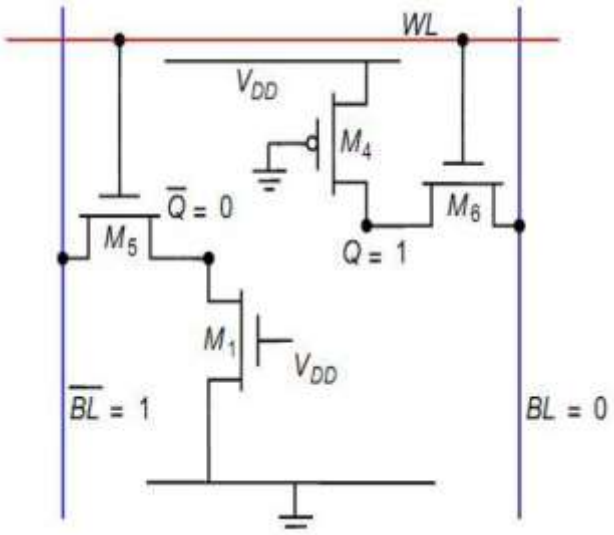


**Figure 6**

### *C. Hold operation*

In hold condition the word line WL is set to off condition that is word line is at 0 , the access transistors M5 and M6 are turned off. Inverters formed by four transistors will be connected to each other giving inverted out put to each one. The inverters are connected hence they retain the memory which was earlier fetched. The data are held in latch.

### DECODERS

Whenever a memory allows for random access- based access, address decoders must be present. The design of these decoders has a substantial impact on the speed and power consumption of the memory. The normal decoder can be built using logic gates. However, the normal built using logic gates may cause several problems. The main problem is that the decoder will require a very large number of transistors. The capacitance associated with the long runs of wires and high gate input count will add to long delays. So we need to design a decoder with less transistors and wires to avoid the delays.

The row address decoder is required to select one of the 2M word line in response to an M bit address input [11]. As an example consider the case M=8 bits and denote the 8 word lines as WL0, WL1, WL2, WL3 _ _ _ _ _, WL127 respectively.

The function of column address decoder is to connect one of the $2^N$ bit lines to the data I/O line of the chip.

A NOR based decoders are implemented for both row and column decoders. The NOR decoder works just like any other dynamic circuit and the design is simple with less wires which results in fast access of data. A NOR based decoder is as shown in figure 7.

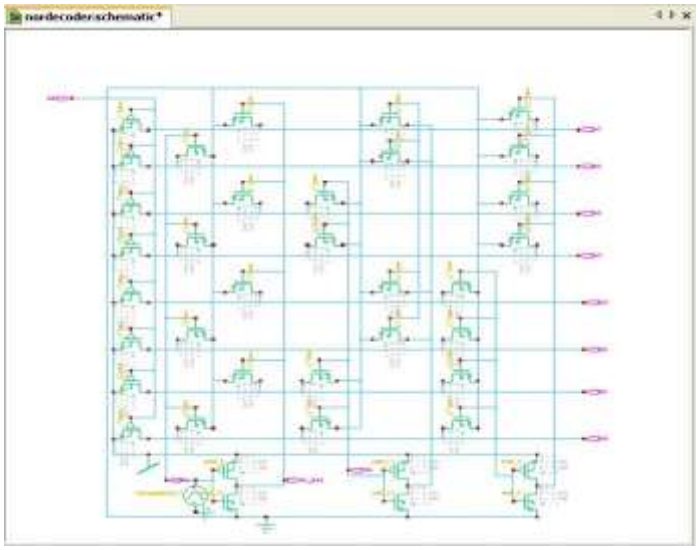

**Figure 7**

### SENSE AMPLIFIER AND PRE-CHARGE OPERATION

The primary function of a sense amplifier in SRAMs is to amplify a small analog differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. A sense amplifier is designed as a differential amplifier. It compares the difference between BL and $\overline{BL}$ and gives the corresponding output. If BL is greater then $\overline{BL}$ the output is high else the output is low. This A SA allows the storage cells to be small, since each individual cell need not fully discharge the bit line .allows the output to set quickly without fully charging or discharging bit line. Figiure 5.a shows the implementation of sense amplifier.

 

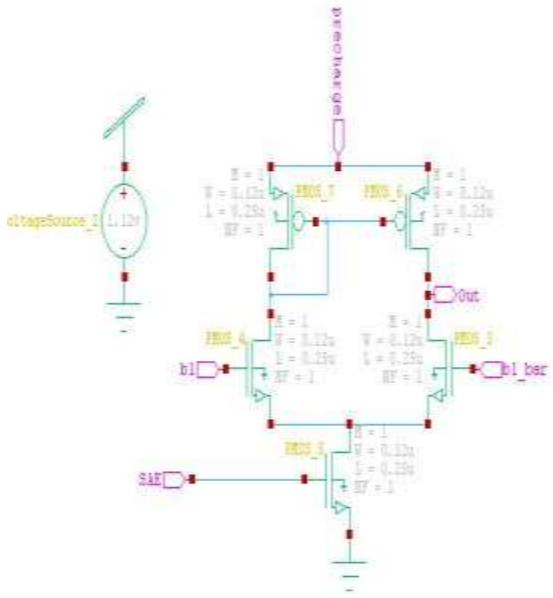


**Figure 8**


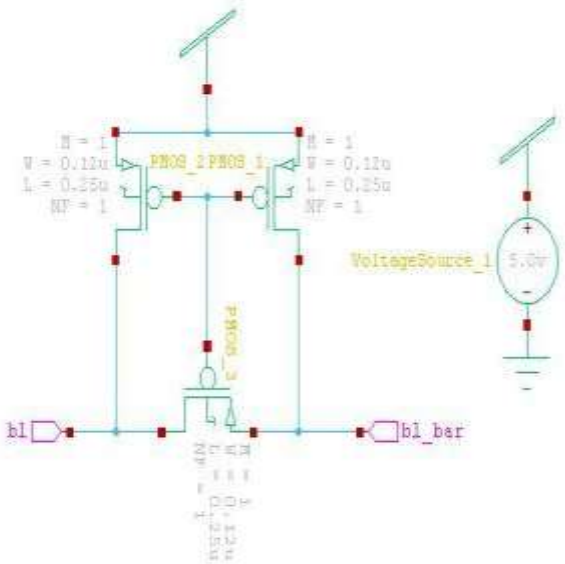


**Figure 9**

## SIMULATION AND RESULTS

The simulation result of decoder is as shown in figure 6.a. In NOR decoder total number of transistor is 38 compare to dcoder implemented by AND gate it uses 54 transistors which makes it bulkier. It shows when all the line are 101 word line wl5 is selected

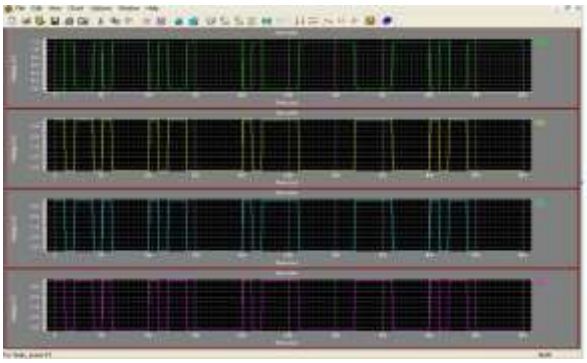

**Figure 10.a simulation result of NOR decoder**

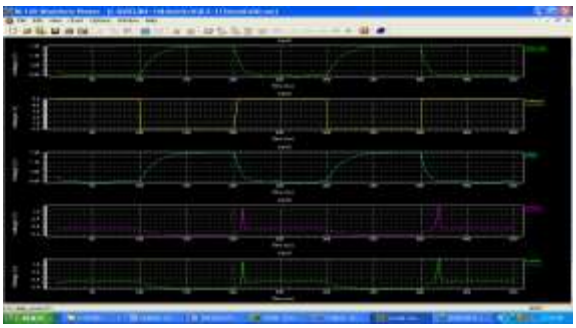

**Figure 11 shows the result of write operation**

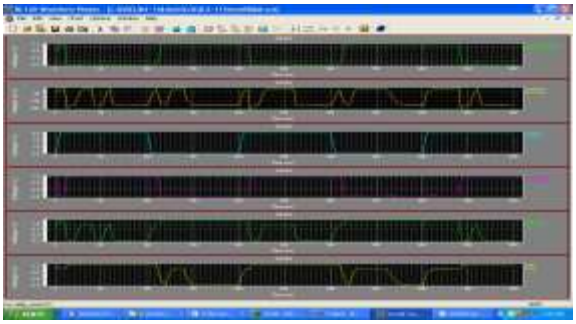

**Figure 12 shows the result of read operation**

The write cycle is the minimum time required between write cycles. The simulations for the WRITE operation of a SRAM cell is shown in figure 6.b

Write access time = 20.76ns - 20.49ns
= 0.27ns

and the read access time is calculated as

Read Access Time = 19.20ns – 18.74ns
= 0.46ns

 

## CONCLUSION

The design and implementation of the SRAM memory is shown in this paper using a negative word line technique. The write access time have been improve effectively from 0.75ns to 0.27ns making it faster in access. The total power consumption also significantly reduced as compared to the existing 6T SRAM memory system.

## REFERENCES

[1] Chua-Chin Wang, senior member IEEE, Ching-Li Lee and Wun-ji Lin " A 4Kb Lowpower SRAM design with negative word-line scheme",vol.5,no.5,May 2007.

[2]. Sung-Mo Kang, Yusuf Leblebici " CMOS Digital Intigrated Circuit-analysis and Design" Tata McGraw-Hill Edition 2003

[3] Andrei Pavlov, Manoj Sachdev" CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies- Process-Aware SRAM Design and Test" springer 2008

[4] E. Seevinck et al., "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE J.Solid-State Circuits*, vol.SC-22, no.5 pp.748-754, Oct. 1987.

[5] Benton H. Calhoun Anantha P. Chandrakasan, "Analyzing Static Noise Margin for Sub-threshold SRAM in 65nmCMOS",*ESSCIRC*,2005

[6] B. Prince, Semiconductor Memories. New York: Wiley, 1991

[7] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic "digital integrated circuits" second edition

[8] Sreerama Reddy G M, P Chandrashekhara Reddy "Design and Implementation of 8Kbits low power SRAM in 180nm technology" IMECS2009, march18-202009, Hong Kong.

[9] L. Chang et al., "Stable SRAM cell design for the 32 nm node and beyond," in *Symp. VLSI Technology Dig.*, Jun. 2005, pp. 128–129

[10] R.J. Baker, H.W. Li, and D.E. Boyce "CMOS-Circuit design, Layout and Simulation".New York Wiley1998

[11] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic "digital integrated circuits"second edition.

[12]. K. Zhang, U. Bhattacharya, Z. Chen, F. Hamzaoglu, D. Murray, N. Vallepali, Y. Wang, B. Zheng, and M. Bohr. A 3-GHz 70-Mb SRAM in 65-nm CMOS technology with integrated column-based dynamic power supply. *IEEE Journal of Solid State Circuits (JSSC)*, 41:146–151, January 2006

 