Design of High Performance 12T SRAM Cell

R. Navajothi[#1] and Dr. A. Kaleel Rahuman*[2]
[1]*PG Scholar and* [2]*Assistant Professor*
[1,2]*Department of Electronics and Communication Engineering*
[1,2]*PSNACET, Dindigul, Tamil Nadu, India*
[1]*navajothirajamanickam@gmail.com*
[2]*kaleelvlsi@psnacet.edu.in*

Abstract: Due to increasing in the need of electronic systems, the number of transistors getting increased in the modern integrated circuits. Most of the systems mainly consist of Static Random Access Memory (SRAM) to store the data and process. In which maximum of total active mode energy is consumed due to leakage current. SRAM array is main source of leakage current since majority of transistor are utilized for on-chip memory in high performance microprocessor and system on chip. Hence there is need to design of low leakage SRAM is required. The main objective is to design and implement 11T and 12T based SRAM cell with less leakage current. The concept of Virtual VDD is employed in 12T-SRAM cell to reduce the leakage. This helps to reduce the dynamic power utilization in the system. Power dissipation of 12T-SRAM cell is less when compared to the existing 11T-SRAM cell by using the 16nm Predictive Technology Model (PTM). The half-select issue is the major problem in SRAM design. The proposed method help the cell to free from the half-select issue. By using Virtual VDD architecture, helps to reduce the leakage current, improve the number of counts of transistor and stability of the system. The average read power consumption reduces approximately 12% compared to the 6T cell due to lower discharging activity at read bit line and low leakage current. But thus 11T structure is less performance compare with 12T SRAM cell.

Keywords: Low power, low voltage, virtual vdd, design methodology, leakage currents.

1. INTRODUCTION

Embedded static random-access memories (SRAMs) overwhelm the power utilization, region, execution, and yield of rising versatile electronic devices. These devices require low vitality utilization to permit long operational lifetimes as they are regularly battery controlled. More than 70 % of the SoC area is occupied by SRAM.As a substantial number of current processors utilize SRAM cells, the speed of their operation has a huge reliance on the speed of SRAM. Other than speed, control utilization, spillage current and range of SRAM assume an imperative part for the processors.

A minimum energy point is reached in the sub threshold region. Thus, it is desirable to operate the cell in the near threshold/sub threshold region. But, several challenges are faced in sub threshold operation. These include essentially corrupted ION/IOFF proportion and vast process, voltage, temperature (PVT) varieties. Sub threshold circuits suffer from threshold voltage (Vt) variation due to random dopant fluctuation (RDF) more acutely as ISUB (drain-to-source sub threshold current) is exponentially dependent on Vt in sub threshold region.

The conventional 6T SRAM cell used in microprocessors has a basic structure and has possesses expansive storage capability but also suffers from half-select disturb and negating read/write requirements. Which has enhanced write capacity however confronts read irritate. In this article, we propose a novel 10T SRAM cell which makes use of the data-dependent stack PMOS switching (DSPS) write help plan to enhance the write capacity and write delay. The proposed outline decouples the read current way from the capacity hub which essentially enhances the read-solidness.

2. EXISTING METHOD

SRAM cells suffer from soft-error issue (likewise called single-event upset). This error implies that the stored datum was incorrect. Emphatically charged alpha particles radiated from packaging materials that contain little measures of radioactive contaminants transports through semi-conductor achieving impact ionization and controlling dispersal of electrons of the limit center points. Its effect is essentially felt in sub edge district in view of the basic charge in the capacity hub being less. The transistors P1, P2, N1 and N2 constitute the cross-coupled inverter latches.

The transistors N5 and N6 are utilized for upgrading the read dependability as the way of the read current is decoupled from the capacity hub. The proposed plan, in this way, has a single-ended read operation. An essential element of the proposed plan is the DSPS write help scheme. Since two distinct plans are utilized to enhance the read soundness and write capacity, the issue of estimating strife for read and write operations as confronted if there should arise an occurrence of the traditional 6T SRAM cell is no more experienced. The transistors MN3 and MN4 are the access transistors and two PMOS transistors P3 and P4 are used as stack transistors.

The PMOS stack transistors are used to implement the DSPS write assist scheme which was explained in detail later in this section. The word-line (WL) is line based and the compose word-line A (WWLA) and compose word-line B (WWLB) are section based. The virtual VSS (VVSS) is line based and is utilized to lessen the impact of leakage current from BL amid the hold mode and for the half chose cells amid read/write by keeping it precharged. The proposed plan uses a single bit line (BL) which is column-based. This work is based on the 45-nm Predictive Technology Model (PTM), in which variety of edge voltage involves concern.

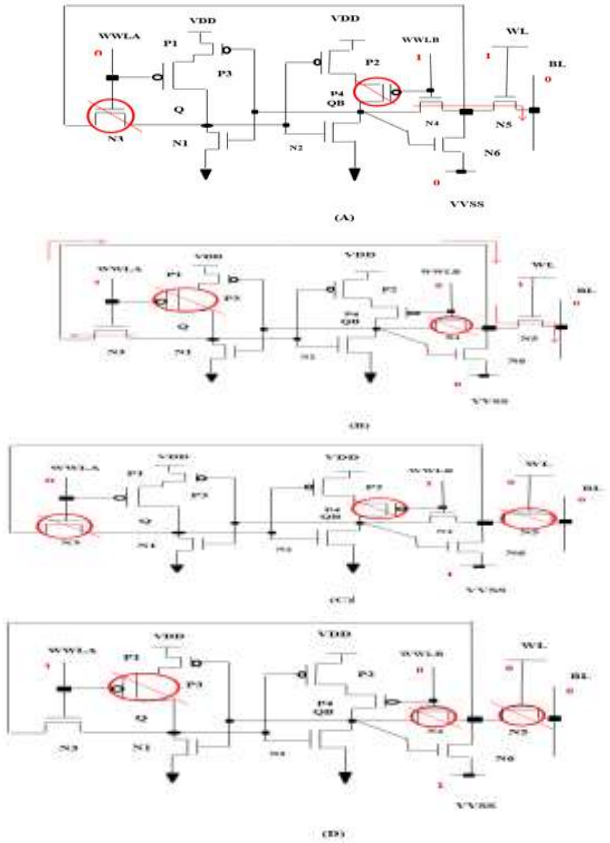

Fig.1 A selected cell under write '1' operation. B selected cell under write '0' operation. C column half-selected cell under write '1'.D column half-selected cell under write '0' operation

Amid the hold mode, WL, WWLA and WWLB are kept grounded. BL was precharged VVSS is also kept precharged to reduce leakage of BL. The transistors N5and N6 are utilized to play out the read operation. Duringread, the chose bit line, BL, is kept precharged.

For the write operation, WL is raised to VDD, BL and VVSS are compelled to ground.The proposed cell uses the DSPS write help strategy. In this segment half-select cell, assume QB (Q) is storing'1' ('0') and WWLB (WWLA) is raised to VDD (grounded). QB won't discover a release way to BL (which is kept grounded) as WL is not charged for an unselected line and VVSS is likewise precharged.

3. PROPOSED SYSTEM

The SRAM cell design having low power and high stability. SRAM design as the demand of the portable electronic market constantly for less power- hungry architectures. It has currently been associate era of moveable electronic devices like mobile phones, iPods, tablets etc. They ought to have an extended battery backup so the devices may be operational for lasting. Major a part of the battery is drained by show and different peripheral parts like speakers. Next to them their memory parts consumes additional power from the battery. Random-access device permits keep knowledge to be accessed directly in any random order. In distinction, different knowledge storage media like laborious disks, CDs, DVDs and storage device, moreover as early primary memory varieties like drum memory, scan and write knowledge solely during a planned order, consecutively, as a result of mechanical style limitations. One has to scale down the feature size of the CMOS devices to meet these objectives.

Technology scaling results in a significant increase in leakage currents in CMOS device. Leakage power consumption is a major contributor for power consumption and has become a serious concern in SRAM cells. In the modern technology when the feature size is reduced drastically, supply voltage and threshold voltage must be also reduced in the same pace. The decrease in power supply reduces the power consumption quadratically at the cost of degraded stability and access delay.The cell stability (read stability plus write-ability) in SRAM cell is studied in detail because it is an important design criterion. The read stability is measured in terms of static noise margin (SNM) which is defined as the minimum noise voltage necessary to flip the state of an SRAM cell.

Therefore, the time to access a given knowledge location varies considerably reckoning on its physical location. Static Random-Access Memory (SRAM) could be a style of semiconductor memory that uses bi-stable latching electronic equipment to store every bit. The term static differentiates it from dynamic RAM (DRAM) that should be sporadically invigorated. SRAM exhibits knowledge remembrance; however it's still volatile within the typical sense that knowledge is eventually lost once the memory isn't steam-powered. For increasing the battery standby time coming up with a replacement style of SRAM cell that consumes less power than the prevailing SRAMs. The key objective behind this proposed design is to cut back the facility consumption of random access memory. During this

proposed design is a unique 12T CMOS SRAM cell is projected.

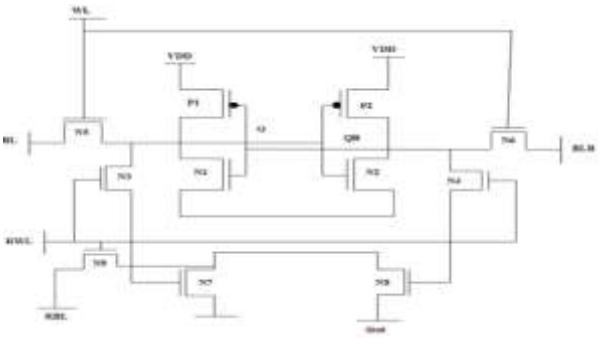

Fig 2. Design Diagram for 11T SRAM

The upper part of the circuit is essentially 6T cell and is used to perform write operation. Transistors NMOS_7, 8 and 9 are used for reading the content of the storage nodes (Q, QB).Read access is single ended and occurs on the separate bit line (RBL). The read word line RWL is distinct from the write word line (WL).To store the data at the storage nodes Q and nQ, the read word line RWL is set to be low. Transistors NMOS_3 and 4 are used to decouple the storage nodes (Q and QB) from read bit line during write operation and standby mode so that proposed cell has distinct write and read ports. Due to separate read and write circuits, the previously stored data remains intact in the cell during next write operation as long as RWL=0.The switching behavior of the transistors NMOS_7 and 8 is decided by the voltage at the storage nodes. Since no current flows between storage nodes and bit lines, the read SNM is almost equal to ideal hold SNM.

The 12T SRAM cell uses separate read and write circuits which improves the read stability of the cell compared to the 9T & 10T cell. Due to no discharging activity for read 1 operation, the read bit line power consumption reduces to 12% as compared to the conventional cell. Due to this intrinsic disturbance, produced by direct-read-access mechanism in the 6T cell, data is more prone to external noise. In the proposed 11-T SRAM cell, read circuit is completely isolated from write circuit which enhances the read stability. This saving can be further improved by proper selection of single ended sense amplifier, decoder and minimum sized transistors. The read delay is degraded by approximately 19% due to use of single ended sense amplifier. Due to larger bit line capacitance and wiring capacitance write power consumption in the proposed cell is increased approximately 6%compared to the 9T & 10T cell.

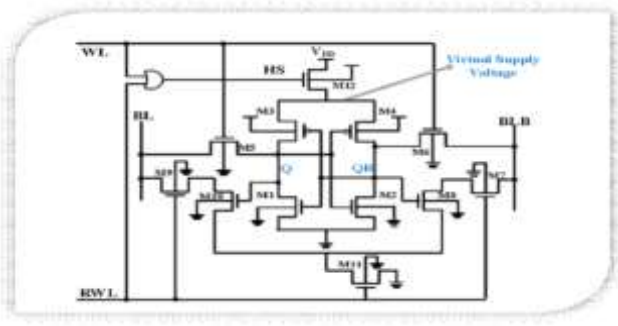

Fig 3. Design Diagram for 12T SRAM

This structure consist of 12 transistors which six main transistors are same as conventional 6T.The four additional transistors respect with 6T are used to separating the read and write path of cell. The cell is single ended structure which does the read operation from one side of cell. Using separated path for read and write operation. That increases the control over the array of the cell in the catch design by simultaneous read and write operations which is in contrast with shared access path as conventional 6T cell. Circuit functionality modes are; Write, read and hold mode.

The WWL and RWL are independent signals and Hold Signal (HS) is produced by them. Both write and read modes are called active mode. For choosing between active and idle (hold) mode, NMOS_1 transistor is used on the top place which separates virtual supply voltage from supply voltage rail. This transistor acts as a power gating transistor. In active mode the NMOS_1 transistor should be in ON mode by producing zero in HS signal (HS=0).After that the write and read operation can be done.

4. MODULE METHODS

(a) SINGLE ENDED READ DECOUPLED SCHEME

Single-ended SRAM (or single bit line SRAM) has gotten to be normal ways to deal with diminish leakage and exchanging force of bit-line (BL).A bit-line usually has a very heavy capacitance loading. Every time a Read/Write operation is performed, the switching of bit-line costs significant power consumption. The single-ended scheme reduces one half of the active power for bit-line switching. A single-ended cell has only one bit-line to carry out the Write operation.

(b) WRITE OPERATION

The write paths proposed design write of two transistors (N5 and N6). In write mode, these transistors actuate with WWL flag and write the estimation of BL and BLB on the capacity hubs. The write operation can be performed at supply voltages as lower voltage. Powerlessness of get to transistors to change the phone's esteem in write operation is called

write disappointment. The transistors P1, P2, N1 and N2 constitute the cross-coupled inverter hooks. The transistors N5 and N6 are utilized for improving the read strength as the way of the read current is decoupled from the storage hub. The transistors N3 and N4 are the get to transistors and two PMOS transistors P3 and P4 are utilized as stack transistors.

(c) READ OPERATION

The read operation is done just from QB stockpiling hub. In this mode RWL flag gets to be one and BL and BBL pre-charge to one. At the point when cell spares the one, (Q=1 and QB=0) the M10 gets to be ON and peruses the Q hub by going the current through N4 and N5.On the other case, when zero is saved in cell (Q=0 and QB=1) the N3 becomes ON and BLB line discharges thorough N2 and N1. In read mode, WL is enabled and VGND is forced to 0 V while remains disabled. The handicapped makes information hubs ('Q' and 'QB') decoupled from bit line amid the read get to. Depending on the cell information esteem, one of the bit lines begins releasing after WL is empowered. In our 10T cell, the read esteem is produced as a transformed flag of cell information and thus, we trade the position of BL and BLB.

(d) TRANSISTORS

In a perfect world, a transistor carries on like a switch. For NMOS transistors, if the information is a 1 the switch is on, else it is off. Then again, for the PMOS, if the information is 0 the transistor is on, generally the transistor is off. Here is a graphical representation of these certainties: When a circuit contains both NMOS and PMOS transistors we say it is actualized in CMOS (Complementary MOS) Understanding the nuts and bolts of transistors, we can now plan a straightforward NOR door. The image VDD is the source voltage (or the rationale 1), GND is the ground (or the sensible 0).

(e) DATA-DEPENDENT STACK PMOS SWITCHING SCHEME

The proposed outline utilizes an information subordinate stack PMOS exchanging write help plot. Because of this element, the cell has enhancements in write SNM and write delays. The proposed outline likewise demonstrates lesser inconstancy in compose postponement and read current on correlation with different cells. The proposed cell indicates higher read current and lower spillage current. In the select case, when the greater part of the beats are stated (and), the NMOS transistors have a full over their entryway to source, the PMOS transistors are off, thus the yield is pulled low.

5. SIMULATION RESULTS (using Tanner EDA tool)

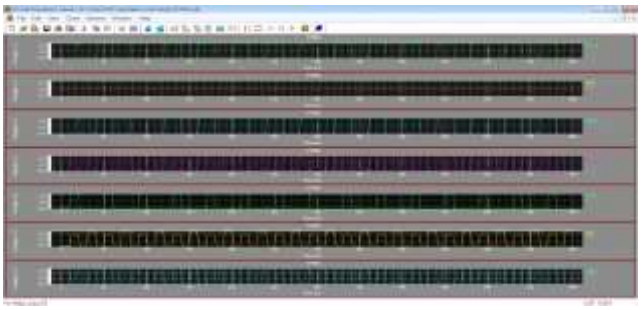

Fig 4: Read Operation for 11T

Fig 5: Read Operation for 12T

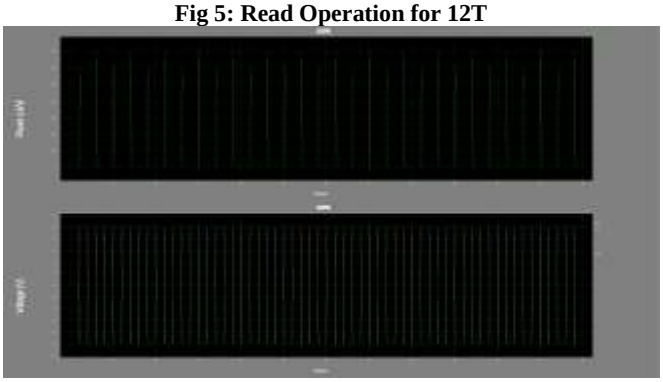

Fig 6: POWER OUTPUT WAVEFORM

Table 1: Comparison Table of 11T & 12T

S.NO	PARAMETERS	OUTPUT VALUE FOR 11T	OUTPUT VALUE FOR 12T
1	POWER CONSUMPTION FOR READ/WRITE	0.705/0.623mwatts	0.230/0.311mwatts
2	SUPPLY VOLTAGE	5V	5V
3	OUTPUT VOLTAGE	AROUND 6V	AROUND 6V
4	TRANSIENT TIME	0.28S	0.25S
5	OVERHEAD	1.52S	1.36S
6	OVERALL TIME	1.80S	1.61S
7	LEAKAGE VOLTAGE	0.593V	0.481V

6. CONCLUSION

This proposed implementation is an 11T and 12T SRAM Cell which is half-select disturb free. The result of 11T and 12T SRAM Cell is compared with 9T and 10T SRAM cell. The design of this low power 11T and 12T SRAM has been proposed which dissipates lesser dynamic power compared to existing SRAM cell. In the proposed design provide low power solution in high speed devices like laptops, mobile phones programmable logic devices etc. The simulation results are less power consumption and dissipation is also less. The proposed 11T & 12T SRAM cell which effectively reduces the both Dynamic and Static power dissipations. The proposed design uses a single-ended read-decoupled scheme because of which, the read current does not flow through the storage nodes. This results in enhancement in read SNM. The proposed cell is also suitable for applications involving low power because as discussed, it dissipates lesser power during read and write conditions as compared to other cells. The effect of temperature on read power has also been demonstrated. Finally, the proposed design possesses higher Thus, the proposed SRAM cell is a good choice as far as fast write and read operation, overall stability of the circuit and meeting low power requirements are concerned.

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