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Execution and Design of Exclusive Gate of Low Power CMOS Design Using Microwind

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***Abstract*—This research project focused on developing innovative low power techniques for large-scale integration (VLSI) logic and memory. Power dissipation is a significant concern when designing a VLSI system. Until recently, dynamic power was the primary concern. However, as technology continues to shrink, static power, which was previously insignificant, has become just as important as dynamic power. As the power consumption of nanoscale silicon VLSI technology increases dramatically, the significance of minimizing leakage power consumption cannot be emphasized enough. A well-known previous technique involves cutting off the vdd and/or gnd connections of transistors to reduce power consumption. However, when transistors are allowed to float, a system may have to wait a long time to reliably restore lost state and thus may experience unexpectedly poor performance. Consequently, maintaining state is vital for a system that necessitates rapid response even when in a dormant state. Our research introduces innovative techniques that minimize power consumption while preserving logical states, making them suitable for systems with extended periods of inactivity but a need for rapid response times. This work contributed to the development of a power and area efficient design for three input xor/xnor gates using CMOS logic. The newly design three input xor/xnor circuit takes less power. All proposed circuit design and power reduction techniques were implemented in the hardware and tested on various three input xor/xnor circuits.**

***Keywords*—CMOS, XOR, NAND, NOR, MICROWIND.**

I. INTRODUCTION

CXOR XNOR gate is a fundamental operating unit in computing and it is used as a basic cell to implement a VLSI model circuit in many processing applications such as multiplier, digital filter, CPU, etc. Therefore, many concepts of Three input XOR/XNOR have been studied in order to reduce the power consumption. A world without electronics cannot be imagined in the present generation. The use of electronic items has encompassed our regular work day to such a degree that it is impracticable to spend a few hours without them. At the outset of the day to its end, we use a brigade of electronic gadgets to enhance various problems solving performance. In sum, we are very dependent on the electronics, as they facilitate our day-to-day routine. For example, the use of mobile phones has changed the definition of communication. The Smartphone was introduced to the public in 1993, with added description like: gaming, email, etc. Instead of physical buttons, the users touch the screen to select the required options. Researchers found that its usage has had a rapid increase from the year 2006 till present. According to recent survey, 77 percent of the world population uses the mobile phone. Also, we use a variety of portable electronic devices which are inbuilt with a variety of operating systems. It is not easy for us to imagine the world without electronic devices.

Digital Signal Processing (DSP) is commonly used in devices such as mobile phones, laptops, multimedia computers, camcorders, CD players, hard drives etc. A DSP chip is a programmable device, which has a set of instructions that enable various algorithms to be coded into it. The adder is one of the key components of a DSP chip. Current devices like microprocessors have become quite powerful with the ability to perform millions of operations per second. As the number of transistors on a chip increases, the power consumption becomes a concern especially for use in portable electronics. Power consumption is one of the top concerns of Very Large-Scale Integration (VLSI) circuit design, for which Complementary Metal Oxide

1.2 Exclusive-Or (XOR) and xnor the fundamental Exclusive-OR (XOR) and Exceptional-NOR (XNOR) gates are of a couple of computerized strategies and are

massively utilized as a part of extremely colossal scale coordination methods reminiscent of equality checkers, comparators, crypto processors arithmetic and common-sense circuit experiment sample mills, especially in Three input XOR/XNOR module as Sum output that is 3-input XOR and many others. In these sorts of projects, XOR and XNOR gats constitute part of the important course of the framework, which significantly influences the most pessimistic scenario stretch and the general execution of the method. An enhanced plan is liked to turn away any corruption on the yield voltage, expend less power, and have substantially less delay in imperative course with sub-micron innovation we profound to scale down low-supply. In our approach, we recognize a fundamental cell phone together with three-input and two outputs. Consequent and if fundamental we rehearse a considerable amount of redress components and enhancement techniques to get adjusted 3-input XOR–XNOR circuits.

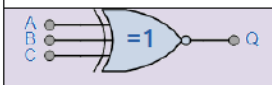
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Then an Ex-NOR function with more than two inputs is called an "even function" or modulo-2-sum (Mod-2-SUM), not an Ex-NOR. This description can be expanded to apply to any number of individual inputs as shown below for a 3-input Exclusive- NOR gate.

3-input Ex-NOR Gate

Giving the Boolean expression of: Q = ABC' + AB'C + A'BC + ABC We said previously that the Ex-NOR function is a combination of different basic logic gates Ex-OR and a NOT gate, and by using the 2-input truth table above, we can expand the Ex-NOR function to: Q = (A ⊕ B) = A'B + AB' which means we can realize this new expression using the following individual gates

Table 1.2 3-input Ex-NOR Gate

Symbol	Truth Table			
 3-input Ex-NOR Gate	C	B	A	Q
	0	0	0	1
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	1
	1	1	1	0
Boolean Expression $Q = \overline{A \oplus B \oplus BC}$	Read as "any EVEN number of Inputs" gives Q			

Static logic is a design methodology in integrated circuit design where there is at all times some mechanism to drive the output either high or low. For example, in many of the popular logic families, such as TTL and traditional CMOS, there is always a low-impedance path between the output and either the supply voltage or the ground. The most widely used logic style is static CMOS. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1(based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0 (based on the inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such that, one and only one of these networks is conducting in the steady state. Dynamic logic is a design methodology in integrated circuit design in that it uses a clock signal in its implementation of combinational logic circuits. In dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used before it leaks out of the capacitance holding that state. The basic construction of a dynamic logic gate is shown in fig.2. The PDN (pull-down network) is constructed exactly as in complementary CMOS. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK.

1.4 Motivation

Power consumption is a key limitation in many electronic systems, ranging from mobile telecom to portable and desktop computing systems. Power is also a show stopper for many emerging applications like ambient intelligence and sensor networks. Consequently, new design techniques and methodologies are needed to control and limit power consumption. From sophisticated handheld devices to bioelectronics circuits and nano-satellites, all require low power design. Due to scaling, circuits are becoming more capable, use more transistors to implement complicated functions and offer new applications to customers. But this means more power consumption. In some cases, low power design is required to avoid overheating. There are other applications like bioelectronics where the circuit would be implanted inside the body and has to work either with small battery or using power harvesting techniques. Similar to that, RFID and growing sensor networking circuits also have to consume very low power because of available power limitation. In some cases, we may consider low-power design a second priority, but in those applications lower-power design is critical. So either source power limitation or, overheating concern and battery life consideration, low power design is the answer.

In digital processing, a three input XOR/XNOR is one of the main elements; an ALU, DSP and digital filtering in any microprocessor/microcontroller are based on it. Therefore, to have low power digital processing, a low power Three input XOR/XNOR is desired. In terms of power reduction techniques and comparison there are few

papers and references available. At the architecture level, some solutions like adiabatic circuits have been introduced to reduce power consumption. However, some of these solutions, like adiabatic, may not be practical due to the number of transistors they require. Some of these techniques like pipeline structures or asynchronous timing becoming more attractive and getting more attention than other solutions. This is beside the original and main solution to reduce the supply voltage.

II. LITERATURE REVIEW

Tooraj Nikoubin et al(2016), We observed that a, SCDM serves as a design methodology for three-input XOR/XNOR, which is one of the most complex and competitive as well as all-purpose three-input basic gates in arithmetic circuits. In the end, three new high performance three-input XOR/XNOR circuits with less PDP and occupied area are conceived using SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay.

Gopal et. al (2016), in these projects two novel design methodologies of low voltage OR-XNOR circuits are tested. The performance of the proposed circuits can operate at low-voltages, and have good output levels. The proposed circuits tested to have noise immunity, higher energy-efficiency and faster operation. In the end, new high performance three-input XOR-XNOR circuits with less PDP and occupied area are designed.

Tung et. al (2013), this paper proposes a low-power, high speed full adder (FA), abbreviated as LPHS-FA, is presented as an elegant way to reduce circuit complexity and improve the performance thereof. Employing as few as 15 MOSFETs in total, an LPHS-FA requires 60-73% fewer transistors than other existing FAs with drivability. For validation purpose, HSPICE simulations are conducted on all the proposed and referenced FAs based on the TSMC 0.18-? m CMOS process technology. The LPHSFA is found to provide a 20.4-21.2% power saving, a 12.3-67.0% delay time reduction and a 35-102% reduction in power delay product compared with the referenced FAs. In short, an LPHS-FA is presented in a concise form as a high-performance in practical applications.

Y Jagadeeshet. al (2013), in this paper we observe that CMOS technology achieving high performance has resulted in increase of leakage power dissipation. It proposed inefficient methodology for reducing leakage power in VLSI design. Our Dual sleep approach shows improved results in terms of static power, dynamic power and power delay product. It gives the CMOS circuit designers another option in designing integrated Circuits more efficiently.

Reddy et. al (2013), This proposed work illustrates the design of the low-power less transistor full adder designs using cadence tool and virtuoso platform, the entire simulations have been done on 180nm single n-well CMOS bulk technology, in virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 100MHz. These circuits consume less power with maximum (6T design) of 93.1% power saving compare to conventional 28T design and 80.2% power saving compare
to SERF design without much delay degradation. The proposed circuits exploit the advantage of GDI technique and pass transistor logic.

III. PROBLEM STATEMENT

This research work addresses new low power approaches for Very Large-Scale Integration (VLSI) logic and memory. Power dissipation is one of the major concerns when designing a VLSI system. Until, dynamic power was the just concern. However, as the technology feature size shrinks, static power, which was minor before, becomes an issue as important as dynamic power. Since static power increases significantly (indeed, even exponentially) in nanoscale silicon VLSI technology, the importance o reducing leakage power consumption cannot be overstressed. A well-known earlier technique called the sleepy transistors technique cuts off Vdd and/or Gnd connections of transistors to preserve leakage power consumption. However, when transistors are authorized to drift, a system may have to wait a long time to reliably restore lost state and thus may experience seriously degraded performance. Therefore, retaining state is critical for a system that requires fast response even while in a stationary (or inactive) state. Our research provides new VLSI techniques that achieve ultra-low leakage power consumption while maintaining logic state, and thus can be used for a system with long inactive times but a fast response time requirement.

IV. PROPOSED METHODOLOGY

4.1 Transient Power Consumption

Transient power consumption is due to the current that flows only when thetransistors of the devices are switching from one logic state to another and this is aresult of the current required to charge the internal nodes (switching current) plus thethrough current (current that flows from VCC to GND when the p-channel transistor
and n-channel transistor turn on briefly at the same time during the logic transition).The frequency at which the device is switching, and the rise and fall times of the input signal, as well as the internal nodes (points) of the device, has a direct effect on theduration of the current spike. For fast input transition rates, the through current of thegate is negligible compared to the switching current. For this reason, the dynamicsupply current is governed by the internal capacitance of the IC and the charge anddischarge current of the load capacitance.

Transient power consumption is calculated using equation 4.

PT = $Cpd \times Vcc$ 2 × FI × NSW (4)

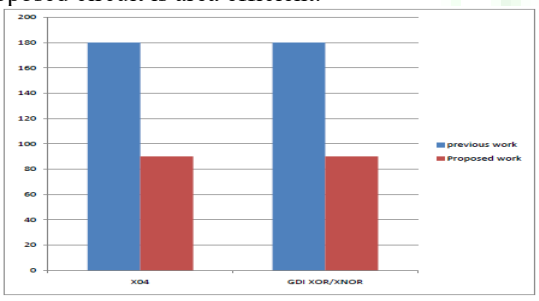
Where:
PT = transient power consumption
VCC= supply voltage
FI = input signal frequency
NSW = number of bits switching
Cod= dynamic power-dissipation capacitance
In the case of single-bit switching, NSW in equation 4 is 1. Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the powersupply rails. Therefore, the power–dissipation capacitance (Cpd) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. Cod is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, Cod can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). Cpd is discussed in greater detail in the next section.

V. Simulation & Result

5.1 Comparison

After going through some previous studies it was decided to take up three circuits: X04, Modified X04 and GDI based XOR/XNOR. These three circuits cover a larger area as well as consume larger amount of power because it is designed in 180 nm. Therefore, a new circuit is proposed which acquires less area and consumes less power.

After comparing the previous work and the proposed work it has been found that the later proves to be more efficient. The table shown below shows that our proposed circuit is area efficient.



Comparison of area

Table 5.1: The power dissipation values

	Circuit	Static Power Dissipation (In Watts)	No. of Transistor
Previous	Modified XO4	2.78E-04	16
	GDI Based XOR-XNOR	1.17E-03	10
Proposed	Modified xo4	4.627888E-10	16
	GDI Based XOR-XNOR	4.934006E-10	10

5.2 Performance Evaluation Parameters

Power dissipation is an open subject in today's VLSI Design field. The goal of existing studies is to establish the accuracy of Xor/Xnor gate circuit and find new improvement methods. The power reduction methods require ground truth as reference. The main drawback of providing such reference is represented by the extra transistors that are needed. We use one approach, dual sleep; this approach reduces the power dissipation of the circuit. Here we concentrate the static power dissipation. So for finding the static power dissipation we use a following formula

Ps= Σ (leakage current) × (supply voltage)

But here we use the HSPICE tool and this tool is simulate the circuit and gives the power dissipation value. So the simulated result of our circuit is shown in the following waveform.

5.3 Experimental Result:

In this section we show a result of the Three Input XOR/XNOR Gate circuits. So table 4.1 shows the static power dissipation values. From the table 4.1, we conclude that previous Three Input XOR/XNOR Gate circuit is taking more power dissipation. Our new design Three Input XOR/XNOR Gate is more efficient than Three Input XOR/XNOR Gate. We can compare the fig .4.2 and fig.4.3 so modify x04 circuit is taking less area because no. of transistor is less. Xor/Xnor gate (XO4). The circuit diagram is shown in the figure 4.5.in fig.4.5, we can see that 16 transistor and 3 inverter is used for designing the X04 circuit .Here we use GDI-type transistors and this circuit is design with the help of DSCH Tool. Then we make a verilog file from DSCH tool then with the help of MICROWIND tool we generate a Layout of the X04 circuit that is shown in the fig.4.6.

Now we go for the output waveform of the Xor/Xnor gate circuits. This output waveform is

Waveforms of Modified XO4 Circuit: From the fig 4.7 waveform of Modified XO4 Circuit we conclude that when input is A=1, B=1, C=0, so output of XOR is 0 and output of

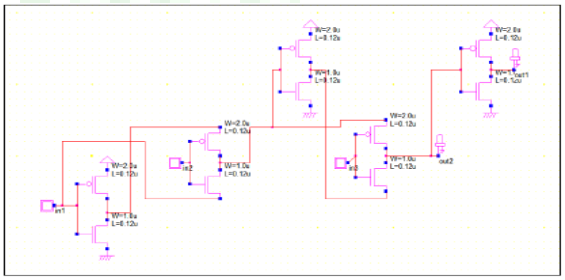


Fig.5.1 Circuit of GDI Based XOR-XNOR Circuit

Waveforms of Modified XO4 Circuit: From the fig 4.7 waveform of Modified XO4 Circuit we conclude that when input is A=1, B=1, C=0, so output of XOR is 0 and output of XNOR is 1. Similarly when input A=1, B=0, C=0, so the output of XOR is 0 and output of XNOR is 1. Similarly when input A=, B=0, C=0, so the output of

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XOR is 1 and output of XNOR is 0. This output waveform is obtained by H-SPICE tool. Also from H-SPICE tool we calculate the power of the circuit.

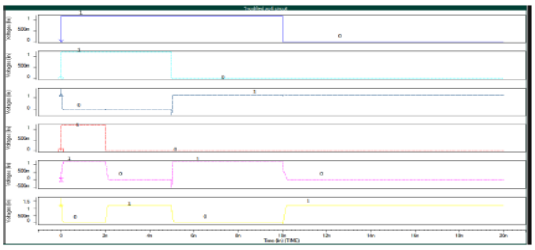

Figure 5.3 Waveforms of Modified XO4 Circuit

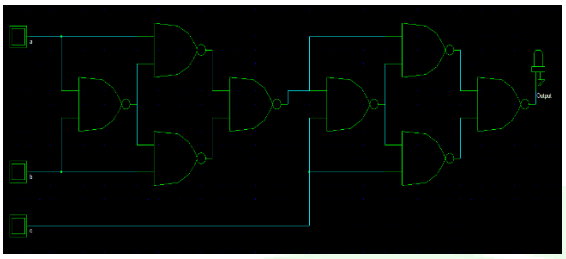

Figure 5.4 Input XOR Gate by Nanad Gate

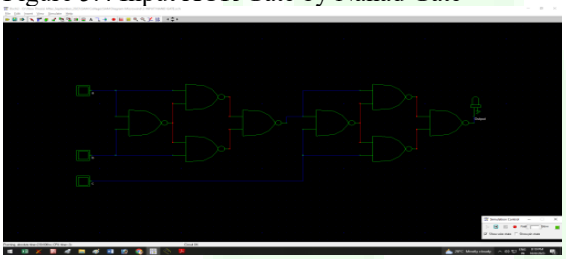

Figure 5.4.a

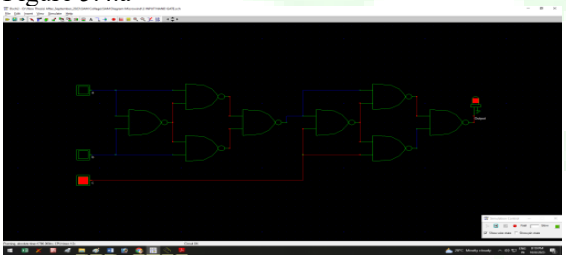

Figure 5.4.b

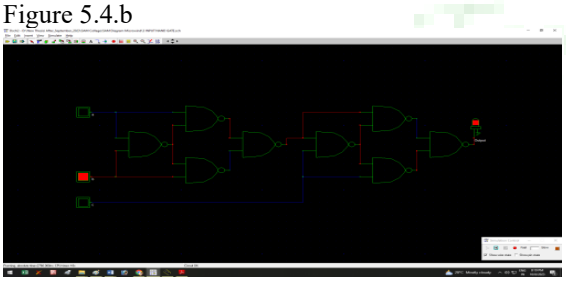

Figure 5.4.c

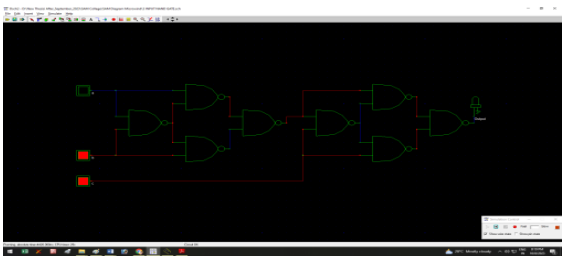

Figure 5.4 d

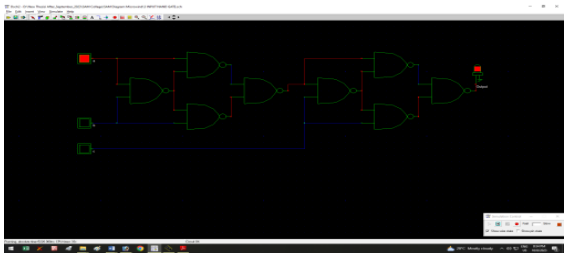

Figure 5.4.e

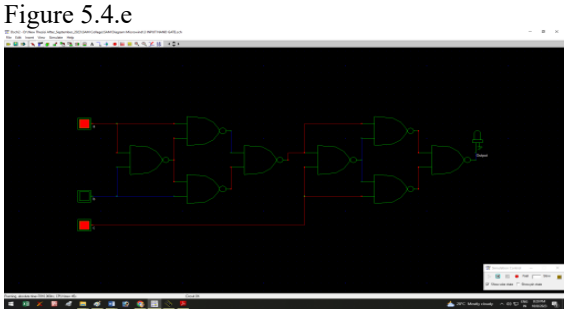

Figure 5.4.f

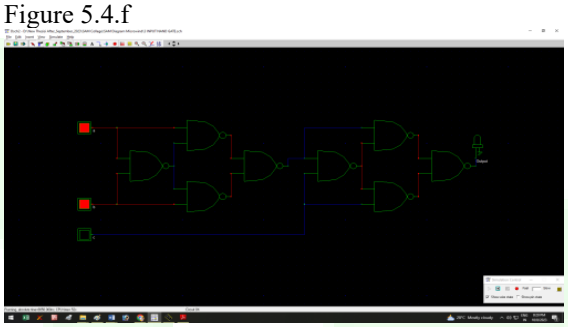

Figure 5.4.g

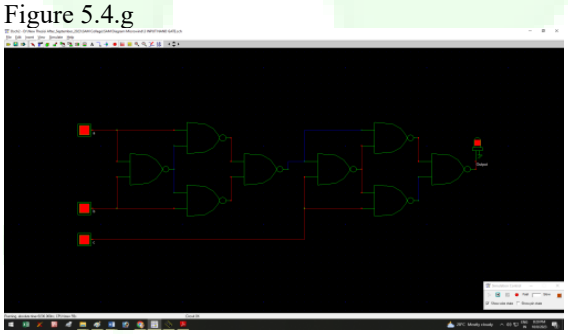

Figure 5.4.h

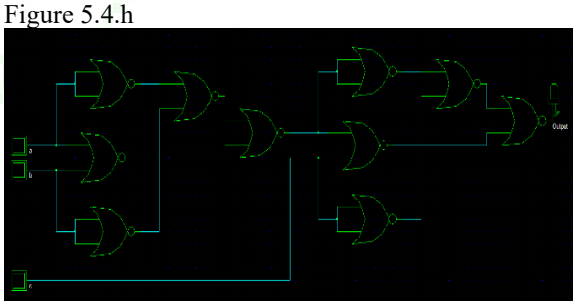

Figure 5.5.3 Input XOR Gate by Nor Gate

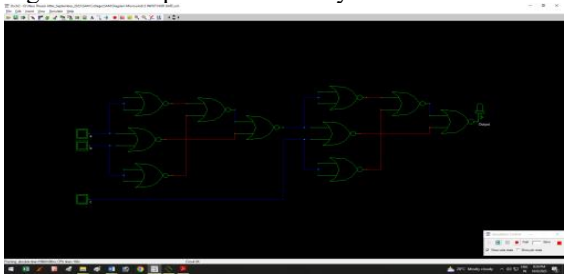

Figure 5.5.a

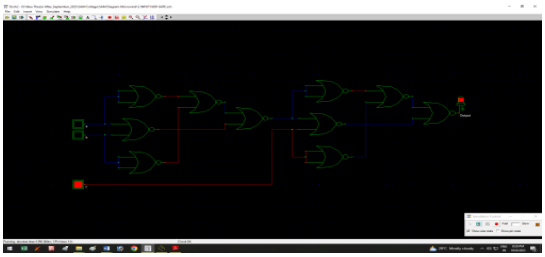

Figure 5.5.b

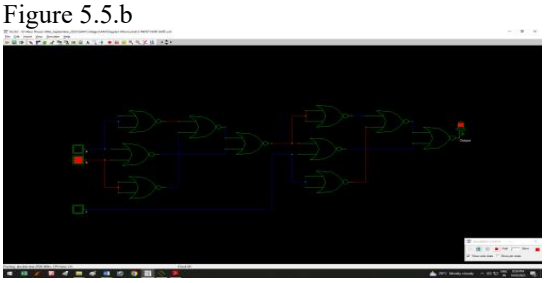

Figure 5.5.c

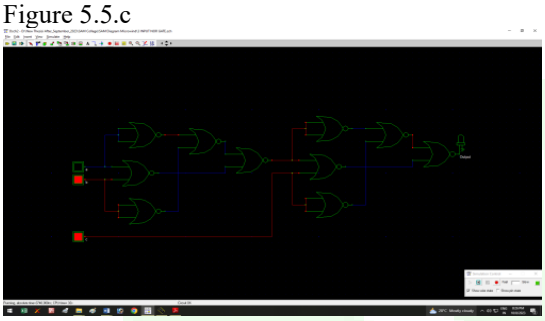

Figure 5.5.d

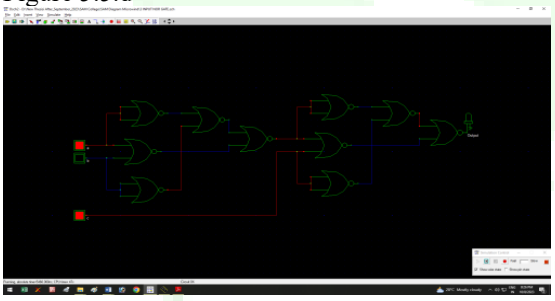

Figure 5.5.e

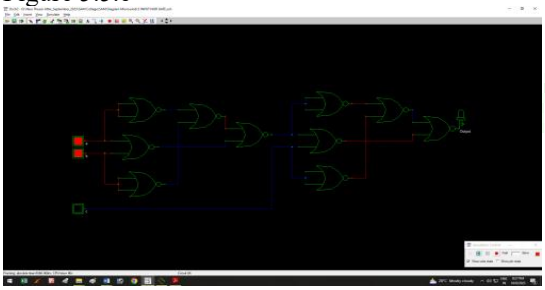

Figure 5.5.f

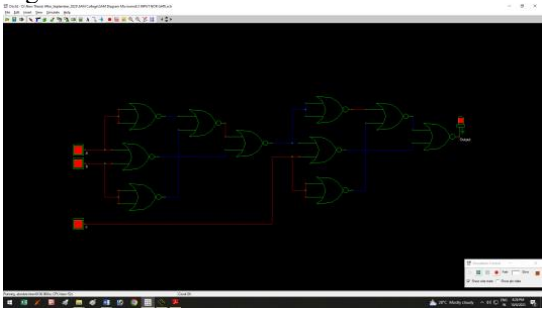

Figure 5.5.g

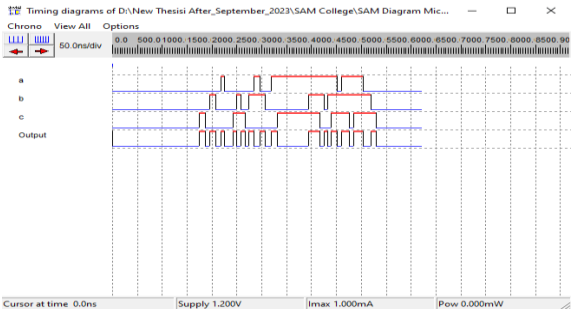

Figure 5.6 Wavefor Result

5. Simulation Result: - Simulation of the circuit csn be simulsted by Microwind Software with efficient power calculation.

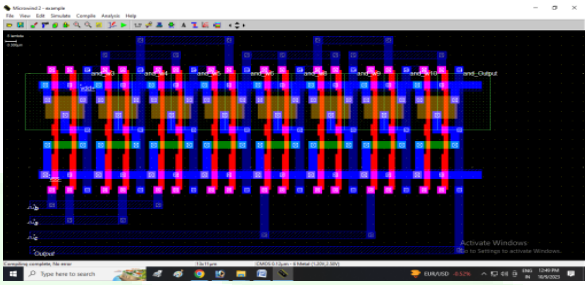

Figure 5.7 Microwind Layout

5.1 Voltege Vs Time Graph:- Volteg Vs Time Graph show in the Figure 4.2. On this simulation power used is 11.189µw.

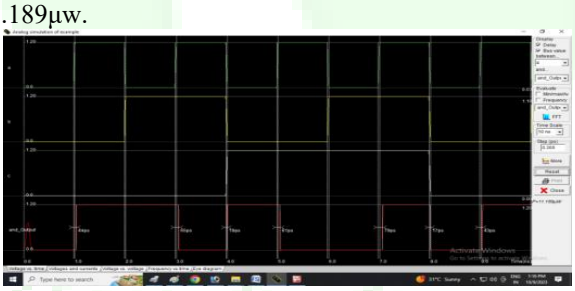

Figure 5.8 Voltage Vs Time Graph

5.2 Voltege Vs Current Graph:- Voltege Vs Current Graph show in the Figure 4.3. On this simulation power used is 9.069µw.

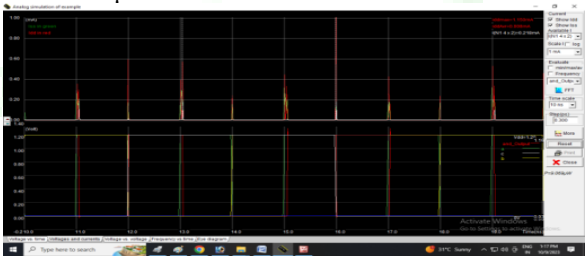

Figure 5.8 Voltege Vs Current Graph

5.3 Voltege Vs Voltage Graph:- Volteg Vs Time Graph show in the Figure 5.8. On this simulation power used is 9.069µw.

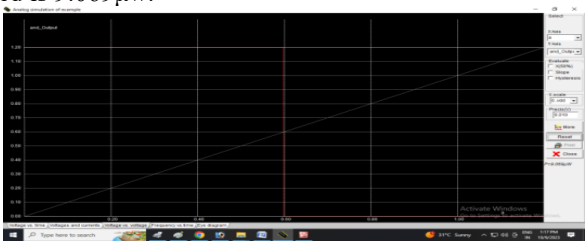

Figure 5.9 Voltege Vs Voltage Graph

5.4 Frequency Vs Time Graph:- Frequency Vs Time Graph show in the Figure 4.5. On this simulation power used is 9.808µw.

Figure 5.10 Frequency Vs Time Graph

5.5 Eye Diagram:- Eye Diagram Graph show in the Figure 4.6. On this simulation power used is 9.808µw.

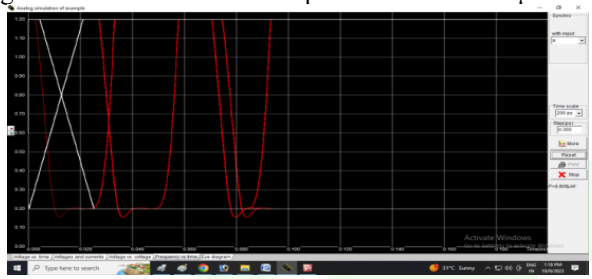

Figure 5.11 Eye Diagram

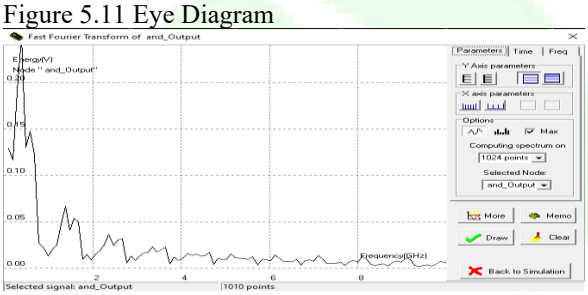

Figure 5.12 FFT Analysis of Circuit

Ratioed logic is an endeavor to diminish the quantity of transistors required to actualize a given rationale work, at the cost of decreased heartiness and additional power scattering. The motivation behind the PUN in correlative CMOS is to give a restrictive way amongst VDD and the yield when the PDN is killed. In ratioed rationale, the whole PUN is supplanted with a solitary unequivocal load gadget that pulls up the yield for a high yield (Figure Rather than a blend of dynamic draw down and pull-up systems, such a door comprises of a NMOS pull-down system that understands the rationale work, and a basic load gadget. demonstrates a case of ratioed rationale, which utilizes a grounded PMOS stack and is alluded to as

VI. Conclusion & Future Scope

Conclusion :- In nanometer scale CMOS technology, sub threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. In this dissertation, a new circuit design named “Low Power and area efficient of Three Input XOR/XNOR Gate Using CMOS Logic Design” to tackle the leakage problem will be discussed.

In this dissertation, a static power reduction technique named “Dual Sleep” is proposed. This technique enables us to reduce the static power consumption in low power CMOS circuit without penalizing in delay or area. This design technique offers the low power CMOS circuit designer’s new armor in their arsenal. A Three Input XOR/XNOR circuit called Low-Power Three Input XOR/XNOR. Our Low-Power Three Input XOR/XNOR provides a new way to save power consumption of a circuit. After designing of Three Input XOR/XNOR is proposed. Here, a heavily researched area: low-power VLSI design For systems spending a large percentage of time in Previous work, typically resulting in approximately two orders of magnitude less leakage power over the best of all prior known state-saving VLSI design approaches is being explored.

Future Scope :-

(1) We have implemented our design in chain of four inverters, 1 bit full subs tractor and SRAM circuit. More tests could be done on ISCAS benchmark\ circuits for further verification.

(2) In our design we tried to keep the area equal to previous cases. Further research could be done to explore design techniques to reduce delay and area as well as static power, hence overall increase of circuit performance.

(3) The proposed circuit is used in ALU to improve the performance. And optimized power dissipation.

(4) The proposed circuit is used in digital signal processing (DSP) and microprocessor to improve the performance.

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