http://www.jctjournals.com ISSN(ONLINE):2278 – 3814

Volume-14, Issue-04, April 2025
JOURNAL OF COMPUTING TECHNOLOGIES (JCT)
International Journal
Page Number: 01-07

Design and Implementation of VLSI Architecture of Multiple Kong Stone Full Adder Circuit with FIR Filter for Efficient Power Estimation

Sonali Soni[1], Prof. Aditya Mishra[2],
M. Tech Scholar [1], Professor & HOD [2],
[1, 2] Vidhyapeeth Institute of Science & Technology (VIST), Bhopal

***Abstract*—With the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. In this thesis, it introduces a novel programmable multiplier architecture using high speed multiplication ancient Vedic math's techniques. A new high speed approach utilizing Vedic multiplier using Kogge Stone (KS) adder for addition has also been incorporated in the same and has been explored. Multiplication is an important function in arithmetic operations. A CPU (central processing unit) devotes a considerable amount of processing time in performing arithmetic operations. Multiplication requires substantially more hard-ware resources and processing time than addition and sub-traction. Digital signal processors (DSPs) are the technology that is omnipresent in engineering Discipline. Fast multiplication is very important in DSPs for digital filter, convolution, Fourier transforms etc.**

This article presents a comparison of high-speed and low-voltage full-adder circuits. Our approach is to build a hybrid full-adder circuit in a single unit. This article also discusses the high-speed conventional all-in-one design that combines most of MOSCAP's functions in a single unit for driving all-electric devices. He also introduced a low-power, mostly functional 1-bit full adder that uses MOS capacitors (MOSCAP) in its architecture. This technology helps reduce power consumption, propagation delay, and digital circuit area while simplifying logic design. Simulation results show that the electronic design is superior to traditional CMOS, TG and hybrid collector circuits in terms of power consumption, delay, performance power delay (PDP) and power delay (EDP). The results after the simulation setup show the superiority of the newly designed general adder circuits over the reported conventional adder circuits. The design was implemented in Cadence Virtuoso Schematic Composer on a UMC 0.18 m process model at 1.8V single-ended supply voltage and simulated on Microwind.

***Keywords*—GDI Adder, Pass transistor, Low Power consumption, High Performance, Hybrid Logic, Transient analysis..**

I. INTRODUCTION

Full adder circuits turns out to be the most major circuit utilized in numerous unpredictable arithmetic operations, for example, subtraction, division, increase, exponentiation and so forth the power utilization of these squares can be decreased by lessening the power utilization of the elemental adder and the diminishment in the power utilization of arithmetic and logical unit drives decrease in power utilization of the general framework The reason for this work is to present low power adder cells which are the key parts of different math circuits. A general decrease in Power Delay Product (PDP) has additionally been gotten through this work.

1.2 Why the Need of Low Power Designs in DSM :- At the framework level, as synchronous execution of microchips, adder cells are the essential module in an assortment of number arithmetic units, for example, Arithmetic Logical Units (ALUs), Ripple Carry Adders (RCAs), multipliers and so forth and these viper cells lie in the basic way. As the general execution of synchronous framework relies on basic way, a considerable measure of work has been done devoted to the change of these essential modules and number arithmetic structures. Adder exhibitions can be essentially enhanced by effective usage of convey spread chain. This should be possible by enhancing structure of 1-bit full viper cell which is the fundamental building piece of adders like convey select or convey skip adders (CSAs)

and also that of swell convey adders (RCAs). Additionally better exhibitions have been gotten by utilizing enhanced quick viper structures like as convey look forward adders and restrictive total adders.

An expansive number of full adders have been outlined by scholarly and research foundations. The generally assessed execution parameters are speed, control dispersal and range. However with the development of versatile and inserted applications, control utilization has been given the primary need concerning circuit and framework execution assessments. Besides, the speed change and lessening of transistor tally has been the point of numerous adder plans. The speed of a full adder circuit dominatingly relies on the length of the basic way in a viper circuit. Longer the basic way, bigger is the convey engendering delay. Fig. 1.1 demonstrates the basic way for convey in multi-bit full adder circuit.

1.3 Low Power Design Requirement

Power Considerations: According to the formula:

$Pdyn=Vdd2.fclk.\alpha nn.cn+Vdd.iscn$

the dynamic power dissipation of a digital CMOS circuit depends on the supply voltage Vdd , the clock frequency fclk , the node switching activities αn , the node capacitances cn, the node short-circuit currents is cn , and the number of nodes n. A reduction of each of these parameters results in a reduction of dissipated power. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency fclk is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

II. LITERATURE REVIEW

B. Annapoorani et al, 2022, The adders are the vital arithmetic operation for any arithmetic operations like multiplication, subtraction, and division. Binary number additions are performed by the digital circuit known as the adder. In VLSI (Very Large Scale Integration), the full adder is a basic component as it plays a major role in designing the integrated circuits applications. To minimize the power, various adder designs are implemented and each implemented designs undergo defined drawbacks. The designed adder requires high power when the driving capability is perfect and requires low power when the delay occurred is more. To overcome such issues and to obtain better performance, a novel parallel adder is proposed. The design of adder is initiated with 1 bit and has been extended up to 32 bits so as verify its scalability. This proposed novel parallel adder is attained from the carry look-ahead adder. The merits of this suggested adder are better speed, power consumption and delay, and the capability in driving. A. Morgenshteinet. et. al., 2002 [1] In this paper author presented a novel technique for improvement of all the parameters which are associated with the circuit like lower power consumption this can be achieved by reducing the transistor count of the circuit therefore author has introduce a technique known as Gate Diffusion Input (GDI). The GDI technique has a huge potential to replace a conventional 28T adder circuit design in terms of area and power consumption of the circuit but circuit suffers from voltage degradation problem. This problem can be eliminated by using hybrid GDI technique.

In Hybrid GDI technique, to improve output voltage level, an additional nMOS transistor can be added with basic GDI cell as shown in Figure 3.7. The nMOS transistor is added because it passes strong „0‟ value. The pair of additional nMOS with pMOS of GDI cell makes a single TG cell. An inverter is used activate pMOS and nMOS of TG cell simultaneously. In this design input B is applied to source of pMOS of GDI/TG cell. Now, for input values of A = 0, B = 0 and A = 0, B = 1, due to inverter before GDI cell, nMOS of GDI cell conducts and it passes strong „0‟ to output. When A = 1, pMOS of GDI/TG cell and nMOS of TG cell conducts simultaneously, hence input B will appear as output without any degradation

Vijay Kumar Sharma et all 2020 Full adder is the heart of any central processing unit that is a core component employed in all the processors. This paper presents a design methodology for full adder circuit with minimum number of transistor i.e. reduced size & reduced area. This is then used to implement 10T full adder design for carrying out summation of bits. The analysis of the developed full adder design is done at room temperature CMOS 90 nm and 180 nm technologies using Micro wind tool 2.6.The result shows the comparison between different CMOS technologies in 90 nm and 180 nm using micro wind tool 2.6 on the design in regards of power dissipation, propagation delay and power delay product. A comparison table shown having power, delay and transistor count based comparison at 90 nm and 180 nm technologies showing delay in time and dissipated Power within the full adder summation circuit design at room temperatures. We will also provide the layout of the full adder design at both technologies. The proposed technique shows 96.66% less power consumption in 90 nm and 93.93% less power consumption in 180nm as compare to base paper hybrid logic design.

Adarsh Kumar Agrawalet. al.,2009 [2], In this paper author presented a full adder design by using GDI technique. In Hybrid GDI based XOR gate, one more GDI cell has been added which is controlled by inverted input gate signal of first GDI cell. Both GDI cell behaves as an inverter for any different input combination of XOR gate. When A = 0, pMOS of GDI cell 1 and nMOS of GDI cell 2 conducts simultaneously. When B = 0, GDI cell 2 acts as an inverter and provides inverted input signal A at output end. It means, for B = 0, A = 0, XOR out is „1‟ and for B = 0, A = 1, XOR out is „0.

III. PROBLEM STATEMENT

The GDI method is a standout amongst the most encouraging logic outline techniques in Adder circuit design. The GDI (Gate Diffusion Input) procedure is a low power rationale plan strategy which empowers usage of an

assortment of complex logical capacities utilizing only two transistors PMOS and NMOS combining all four transistors generate EXOR gate. This system is fitting for outline of low power, fast circuits while utilizing few number of transistors (when contrasted with CMOS and other existing methods). The primary inconvenience of the GDI adder is loss of voltage swing which reduces the driving ability of the GDI Adder circuit.

The Pass Transistor Logic (PTL) likewise turns out to be an effective approach to configuration circuits planned for low power applications were minimum no of transistor is required. With the forceful scaling of the transistor estimate because of developing technology, the significance of pass transistor logic has expanded immensely; it is because of the lower hub capacitance acquired in the PTL when contrasted with the node capacitance in CMOS circuit design. The few transistors for the execution of PTL plans are gotten by quickly diminishing the channel lengths of the transistors. The few parameters which is measured help the transistors in lessening the drop (IR drop) across the circuit. Because of these qualities, PTL union turns into a reasonable rationale plan procedure for doing low power, territory effective outlines to meet the necessities of quickly developing electronic industry.

3.1 Complementary Metal Oxide Semiconductor Technology in DSM (CMOS)

The ordinary CMOS outline system is the most essential circuit plan procedure in CMOS innovation which has lower power consumption than other technology. This strategy of making CMOS technology by uses two corresponding arrangements of systems to be specific the "pull up" system and " pull down" system the pull up system is made out of PMOS transistor to pass low level signal to charge the load capacitance and the correlative pull down system is made out of the NMOS transistor which help in discharge the system towards ground. The fundamental structure of a plan in the tradition CMOS outline method is appeared in the Fig. 2.1. In the below figure CMOS circuit consist of system of PMOS and NMOS transistors to charge and discharge the output load capacitance, the C-CMOS configuration uses measure up to number of PMOS and NMOS transistors regardless of the necessity of the plan.

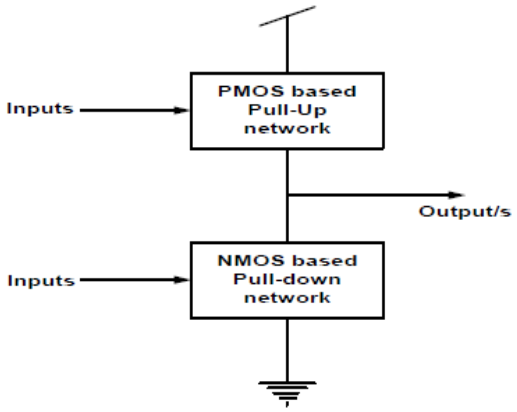


Fig. 3.1 CMOS design

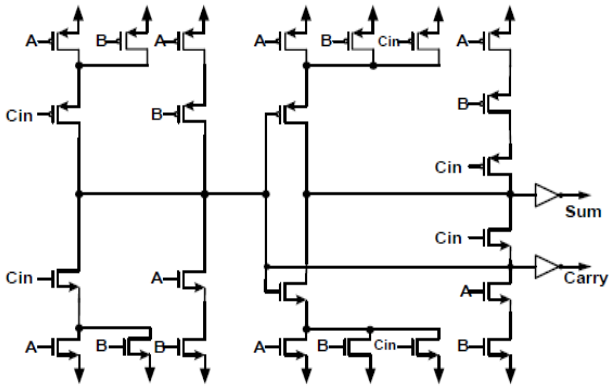


Fig. 3.2 Conventional circuit structure for complementary MOS (CMOS) adder

As the outline recommends the CMOS full adder comprises of 28 transistors with standard CMOS structure both PMOS and NMOS transistor are utilize to form a CMOS structure for saving the power consumption in the circuit, by using this type of technique the voltage swing achieved by the adder circuit is proper. One of its primary benefits is its heartiness against voltage scaling and transistor 28

during scaling of the technology. The correlative plan prompts exceptionally straightforward circuit of a full adder design.

IV. Proposed Methodology

The outline of low power with fast digital framework is the prime test for VLSI originators yet a few imperatives dependably exist for the plan of low power frameworks. So one generally needs to make exchange offs to acquire a framework with preferred attributes and numerous choices exist that make exchange offs between speed of the circuit, oxide thickness of transistor, programmability of the device, and different factors which help in improving overall performance of the circuit. Each processor has Arithmetic Logic Unit (ALU) to play out the math operations required to run the process and adder circuit is a basic circuit utilized for all operations which is performed by an ALU of the processor. The mitigation of power dissipation of adder circuit results in overall mitigation of power in ALU block of the processor.

4.1 Conventional Full Adder Circuit

A full adder is a logical circuit that delivers the expansion of two numbers in a number-arithmetic framework. A one bit full adder circuit addition by using the input A, B, Cin and generate two output known as S and. The full adder comprises of three sources of info (two present bits and one past convey bit) and two yields to be specific whole and convey. Reality table for a full adder circuit is appeared in table 4.1.

Table 4.1 Truth table of full adder circuit design

A	B	C	Sout	Cin
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean operation for full adder outputs can be calculated by using EXOR gate

From the above conditions, which is shown in Fig.4.1. For manufacturing full adder circuit we require two XOR gate s, one NAND gate which is minimum number of transistor are used but in Fig.4.1 two AND, OR gate is extra require. This is the most essential type of usage of a adder circuit albeit diverse type of execution is utilized at the circuit level which fluctuates from configuration to plan.

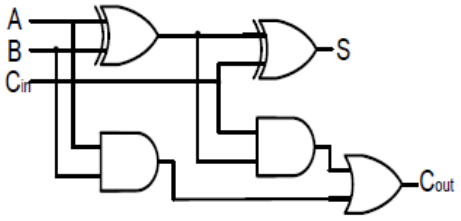


Fig. 4.1 One Bit Full adder circuit design

V. SIMULATION & RESULT

5.1 Introduction

All the existing and proposed circuit Schematic is made by using Cadence Virtuoso schematic proofreader apparatus tool. The schematic graphs of XOR and XNOR based full adder circuits have been appeared in Fig.4.1 and 4.2 separately. These schematic graphs of all adder circuits have been planned and recreated at 180nm and 65nm technology having a supply voltage at 1.8V and 1V respectively.

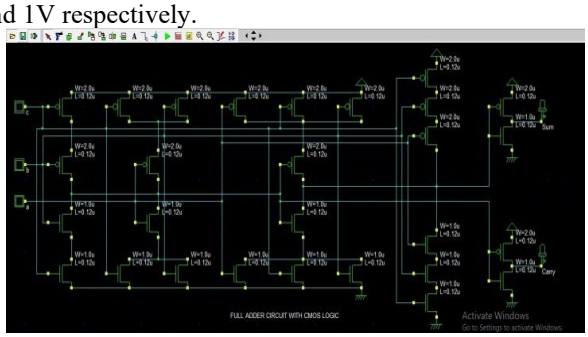
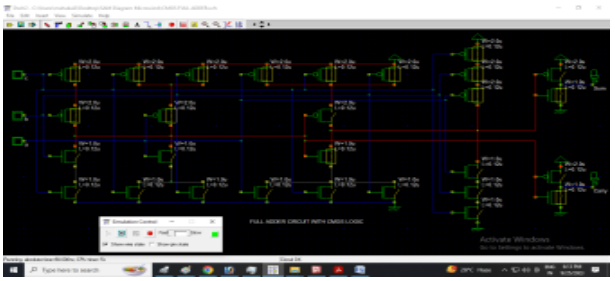
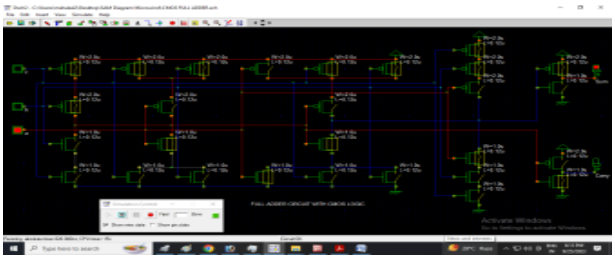
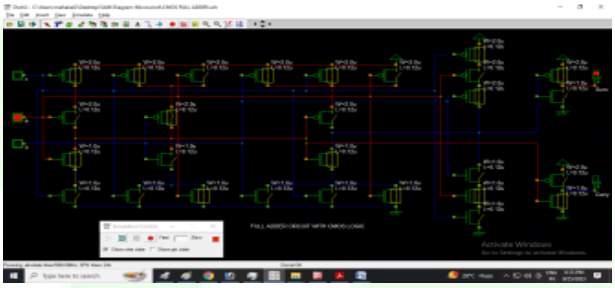
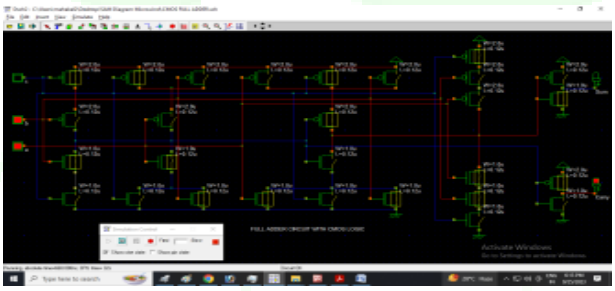


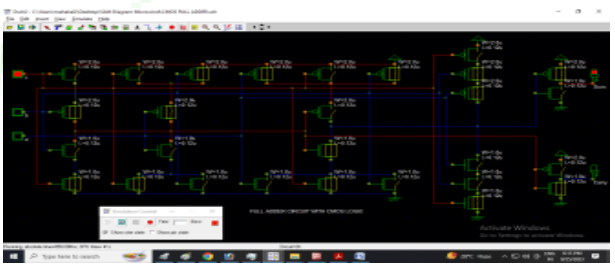
Figure 5.1 28T-Diagram

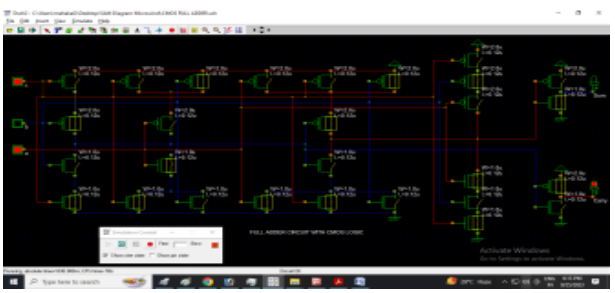


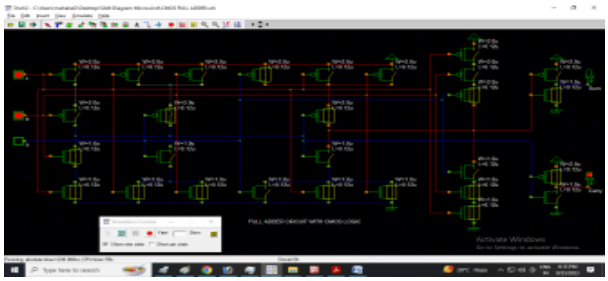












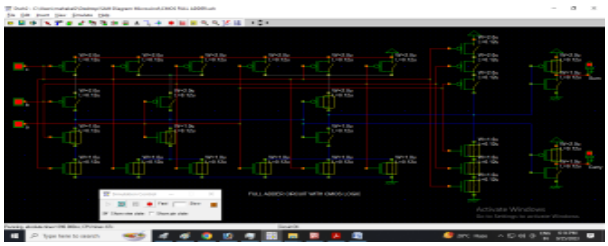


Figure 5.3 Simulation Result

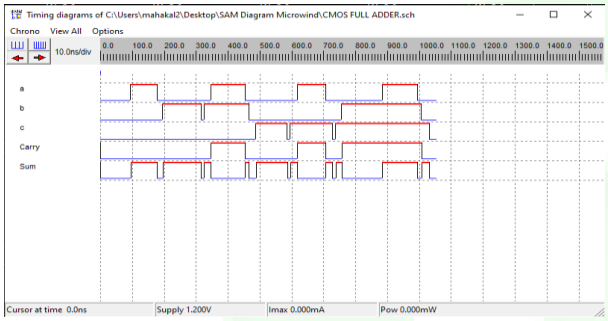


Figure 5.3 Simulation Result Waveform Diagram

5.2 Microwind Result

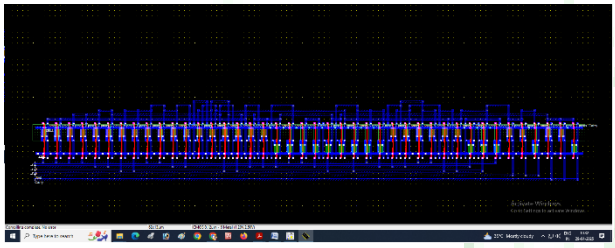


Figure 5.4 Microwind Layout Diagram of Full Adder

5.2.1 Microwind Result at 10ns

5.2.1 Voltege Vs Time Graph: - Volteg Vs Time Graph show in the Figure 5.5. On this simulation power used is 28.878µw.

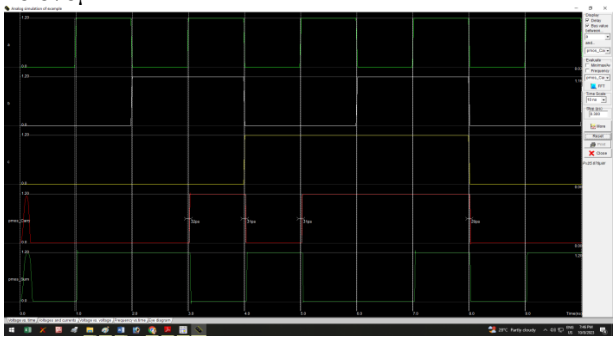


Figure 5.5 Voltage Vs Time Graph

5.2.2 Voltege Vs Current Graph: - Voltege Vs Current Graph show in the Figure 5.6. On this simulation power used is 19.975µw.

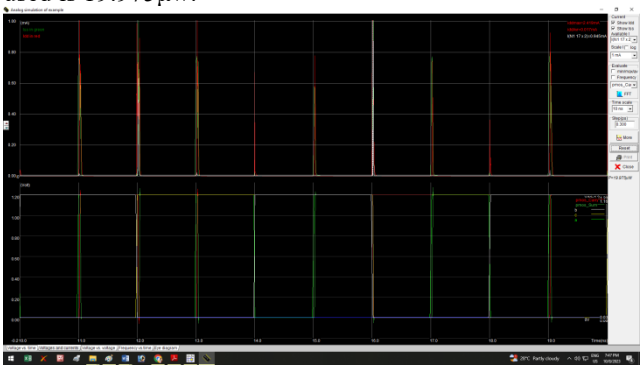


Figure 5.6 Voltege Vs Current Graph

5.2.3 Voltege Vs Voltage Graph: - Volteg Vs Time Graph show in the Figure 5.7. On this simulation power used is 22.828µw.

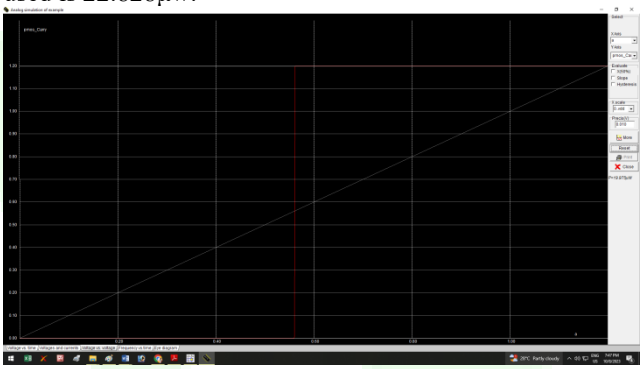


Figure 5.7 Voltege Vs Voltage Graph

5.2.4 Frequency Vs Time Graph:- Frequency Vs Time Graph show in the Figure 5.4. On this simulation power used is 22.828µw.

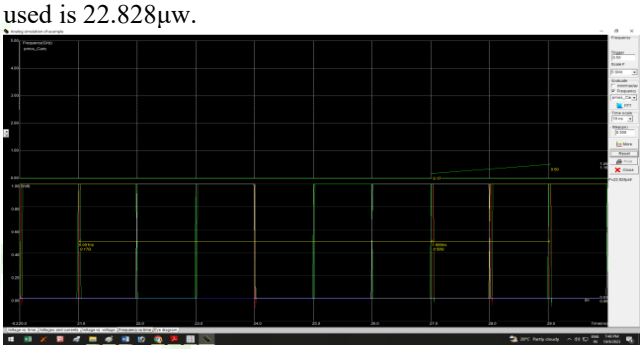


Figure 5.8 Frequency Vs Time Graph

5.2.5 Eye Diagram: - Eye Diagram Graph show in the Figure 5.9. On this simulation power used is 10.196µw.

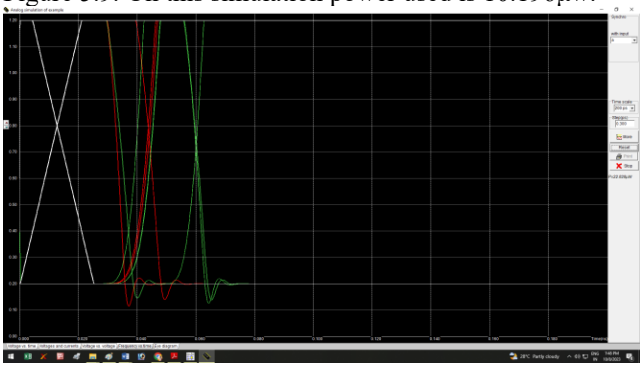


Figure 5.9 Eye Diagram

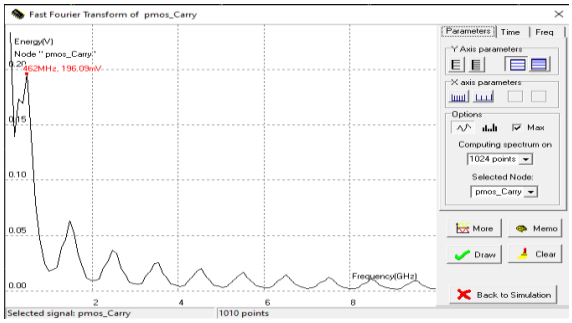


Figure 5.10 FFT Analysis of Circuit

VI. Conclusion & Future Scope

6.1 As we discuss in previous chapters for both existing and proposed circuit it is concludes in over both proposed 13T Hybrid GDI full adder circuits shows better performance in terms of lower power consumption in DSM circuits, provides lower delay to the circuit and over all there is improvement in Power Delay Product (PDP) than all the existing full adder circuits and proposed XOR and XNOR based circuits which is free from the degradation of the voltage level problem with all the existed circuits when compared with proposed circuit. We have compared all the existing adder circuits with the proposed from the simulation results it is observed that proposed circuits has better performance than other existing adders circuit in terms of power consumption of the circuit, propagation delay of the circuit and overall PDP. In over proposed circuit which is made from XOR single bit GDI hybrid adder circuit which shows maximum saving of power 53.2 % when comparison with existing 16T hybrid adder, maximum reduction propagation delay a maximum of 93.4 % in conventional 28T CMOS adder and the maximum PDP is achieved 96.8% in comparison to conventional 28T CMOS adder while. In proposed XNOR based full adder circuits saves maximum reduction of power upto 56.7 % when compared with to the existing 16T hybrid adder circuit, reduction of delay a maximum of 93.5 % when compared with conventional 28T CMOS adder and maximum saving of PDP upto 97.1 % compared with conventional 28T CMOS adder at lower frequency range upto 100 MHz. As we scale down the technology at 65 nm, The proposed XOR based full adder cell circuits saves the power upto 85.2 % when compared to the existing SERF adder circuit, reduction in delay upto 93.4 % when compared with SERF adder and maximum saving of PDP upto 99 % in comparison to SERF adder. The XNOR based proposed single bit full adder cell circuits produce reduction in power consumption a maximum of 86.8 % in comparison to the existing SERF adder, produces reduction in delay a maximum of 93.7 % in comparison to the SERF adder and a huge reduction in PDP a maximum of 99.2 %in comparison to SERF adder at 100 MHz frequency.

REFERENCES

[1.] Deepak Kumar Patel, Raksha Chouksey and Dr. Minal Saxena, “Design of Fast FIR Filter Using Compressor and Carry Select Adder”, 2016 3rd International Conference on Signal Processing and Integrated Networks (SPIN).

[2.] Basant Kumar Mohanty, and Pramod Kumar Meher, “High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 78, No.06, April 2016.

[3.] K. Durga and Mrs. A. Sivagam, “Efficient Adaptive RLFIR Filter based on Distributed Arithmetic Logic Using Reversible gates”, International Conference on IEEE 2016.

[4.] Indranil Hatai, Indrajit Chakrabarti, and Swapna Banerjee, “An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multi-standard DUC”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 23, No. 6, June 2015.

[5.] S. Padmapriya and Lakshmi Prabha V., “Design of a power optimal reversible FIR filter for speech signal processing”, International Conference, pp. 01-06, ICCCI 2015.

[6.] VahidForoutan, MohammadRezaTaheri, KeivanNavi, and ArashAziziMazreah, “Design of two Low-Power full adder cells using GDI structure and hybrid CMOS logic style”, INTEGRATION, the VLSI journal, vol. 47, pp.48–61, 2014.

[7.] Partha Bhattacharyya, BijoyKundu et.al. “ Performance Analysis of Low Power High Speed Hybrid 1-bit full Adder circuit” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, Vol. 23, no. 10, pp. 2001-2008, 2015.

[8.] NabiallahShiriAsmangerdi, JavadForounchi, KureshGhanbari,“A New 8- Transistors Floating Full-Adder Circuit”,20th Iranian Conf. Electrical Engineering, (ICEE2012), May-2012.

[9.] P. M. Lee, C. H. Hsu and Y. H. Hung, “Novel 10-T full adders realized by GDI structure”, Proc. on Intl. Symp. On Integrated Circuits (ISIC2007), pp. 115-118, 2007.

[10.] Basant K. Mohanty, And Pramod Kumar Meher, “A High-Performance Energy- efficient Architecture For FIR Adaptive Filter Based On New Distributed Arithmetic Formulation Of Block LMS Algorithm”, In IEEE Transactions On Signal Processing, Vol. 61, No. 4, February, 2013.

[11.] Pallavi Saxena, Urvashi Purohit, Priyanka Joshi, “Analysis of Low Power, Area Efficient and High Speed Fast Adder”, In International Journal Of

Advanced Research In Computer And Communication Engineering, Vol. 2, Issue 9, September 2013.

[12.] H. Thapliyal, N. Ran-Ganathan and S. Kotiyal, "Design of Testable Reversible Sequential Circuits", IEEE Transactions on VLSI, pp. 1-9, 2012.

[13.] M. Chuang and C. Wang, "Reversible sequential element designs", Proceedings of the IEEE Asia and South Pacific Design Automation Conference, pp. 420-425, 2007.

[14.] G. Challa Ram and D.Sudha Rani, "Area Efficient Modified Vedic Multiplier", 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT).

[15.] S. P. Pohokar, R. S. Sisal, K. M. Gaikwad, M. M. Patil and Rushikesh Borse, "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics", International Conference on Industrial Instrumentation and Control (ICIC) College of Engineering Pune, India, PP. No. 01-06, 2015.

[16.] G. Gokhale and P. D. Bahirgonde, "Design of Vedic Multiplier using Area- Efficient Carry Select Adder", 4th IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2015), Kochi, August10-13, 2015, India.

[17.] G. Gokhale and Mr. S. R. Gokhale, "Design of Area and Delay Efficient Vedic Multiplier Using Carry Select Adder", 4th IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI- 2015), Kochi, August 10-13, 2015, India.

[18.] Sushma R. Huddar and SudhirRao, Kalpana M., ― Novel High Speed Vedi Mathematics Multiplier using Compressors ‖ , 978-1 - 4673-5090-7/13/$31.00 ©2013 IEEE.

[19.] Jucemar Monteiro, José Luís Güntzel, Luciano Agostini "A1CSA: An Energy-Efficient Fast Adder Architecture for Cell- Based VLSI Design", in IEEE Conference, pp 442-445, 2011.

[20.] H. Thapliyal and N. Ranganathan, "Design of reversible latches optimized for quantum cost delay and garbage outputs", Proceedings of the Twenty Third IEEE International Conference on VLSI Design, pp. 235-240, 2010.

[21.] Chandu, H. S. "A Survey of Memory Controller Architectures: Design Trends and Performance Tradeoffs." Int. J. Res. Anal. Rev 9, no. 4 (2022): 930-936.

[22.] Chandu, Hiranmaye Sarpana. "Advancements in Asynchronous FIFO Design: A Review of Recent Innovations and Trends." International Journal of Research and Analytical Reviews 10, no. 2 (2023): 573-580.

[23.] Chandu, H. S. "A Survey of Semiconductor Wafer Fabrication Technologies: Advances and Future Trends." Int. J. Res. Anal. Rev 10, no. 04 (2023): 344-349.

[24.] Chandu, Hiranmaye Sarpana. "Enhancing Manufacturing Efficiency: Predictive Maintenance Models Utilizing IoT Sensor Data." International Journal of Scientific Research and Technology (IJSART) 10, no. 9 (2024).

[25.] Chandu, Hiranmaye Sarpana. "Efficient Machine Learning Approaches for Energy Optimization in Smart Grid Systems."

[26.] Chandu, Hiranmaye Sarpana. "Performance Evaluation of AMBA-3 AHB-Lite Protocol Verification: Techniques and Insights." International Journal of Advanced Research in Science, Communication and Technology (2024).

[27.] Chandu, Hiranmaye Sarpana. "A Review of IoT-Based Home Security Solutions: Focusing on Arduino Applications." TIJER–Int. Res. J 11, no. 10: a391-a396.

[28.] Chandu, H. S. "A Review on CNC Machine Tool Materials and Their Impact on Machining Performance." International Journal of Current Engineering and Technology 14, no. 5 (2024): 313-319.

[29.] Chandu, Hiranmaye Sarpana. "Advanced Methods for Verifying Memory Controllers in Modern Computing Systems." International Journal of Advanced Research in Science, Communication and Technology 4, no. 2 (2024): 377-388.

