http://www.jctjournals.com ISSN(ONLINE):2278 – 3814

Volume-11, Issue-01, January 2022
JOURNAL OF COMPUTING TECHNOLOGIES (JCT)
International Journal
Page Number: 01-07

Design & Implementation FPGA For 2-Bit Comprehensive Golay Code for Error Correcting Parallel Decoder Applications

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***Abstract*— This dissertation presents FPGA Implementation of binary extended Golay Code for Error Correcting Parallel Decoder Applications, which outperform the existing architectures in terms of speed and throughput. The proposed architectures were simulated and tested on Virtex-5 platform. Although the CRC encoder and decoder is intuitive and easy to implement, and to reduce the huge hardware complexity required. The proposed method it improve the transmission system performance level. Implementation and simulation is done using xilinx ISE 14.7 software, ISim simulator is used for validate results in the xilinx test bench. The proposed golay code gives the better performance in terms of the calculated parameters. The proposed golay code optimized the (24,12,3) to (24,12,6) level. The optimized area or component is 318 (6.6 %) while previously it was 493. The delay or latency value is 1.599ns while it was 3.11 ns in existing work. The optimized power is 0.45 mw while previous it is 0.76 mw. Proposed technique is to reduce the circuit complexity for data transmission and reception process. Channel coding is commonly incorporated to obtain sufficient reception quality in wireless mobile communications transceiver to counter channel degradation due to inter-symbol interference, multipath dispersion, and thermal noise induced by electronic circuit devices. High speed and high throughput hardware for encoder and decoder could be useful in communication field. Due to the channel achieving property, the GOLAY code has become one of the most favorable error-correcting codes.**

***Keywords*— VLSI,PDA,FLIP-FLOP,LFSR,GLOAY CODE,ADG,ERROR.**

I INTRODUCTION

The energy demand in our country is rising due to an expAll error-detection and correction plans add some repetition (i.e., some additional information) to a message, which collectors can use to actually look at consistency of the conveyed message, and to recuperate information that not really set in stone to be tainted. Error-detection and correction plans can be either orderly or non-deliberate. In a precise plan, the transmitter sends the first information, and joins a decent number of actually take a look at bits (or equality information), which are gotten from the information bits by some deterministic calculation. If by some stroke of good luck error detection is required, a recipient can essentially apply similar calculation to the got information bits and contrast its yield and the got really take a look at bits; if the qualities don't coordinate, an error has happened sooner or later during the transmission. In a framework that utilizes a non-precise code, the first message is changed into an encoded message conveying the very data and that has essentially however many bits as the first message. Great error control execution requires the plan to be chosen dependent on the qualities of the correspondence channel. Normal channel models incorporate memoryless models where errors happen arbitrarily and with a specific likelihood, and dynamic models where errors happen basically in explodes. Thusly, error-identifying and amending codes can be for the most part recognized arbitrary error-distinguishing/revising and burst-error-identifying/remedying. A few codes can likewise be reasonable for a combination of irregular errors and burst errors. On the off chance that the channel qualities not set in stone, or are exceptionally factor, an error-detection plan might be joined with a framework for

retransmissions of incorrect information. This is known as programmed rehash demand (ARQ), and is most strikingly utilized in the Web. A substitute methodology for error control is crossover programmed rehash demand (HARQ), which is a mix of ARQ and error-correction coding.

1.1 OVERVIEW OF GOLAY CODE

The Golay codes were first found by Golay in 1949. The 23-bit Golay code is an extremely helpful code, especially for those applications when an equality bit is added to each word to yield a half-rate code. Among them, the Golay code was used to give error control on the explorer mission. An arithmetical deciphering calculation for the Golay code is given to address the three potential errors. In 1990, another disentangling approach created is created, called the shift-search unraveling strategy. As displayed, this shift-search technique contrasts well in intricacy and speed and the totally Elia deciphering strategy. The mathematical method is somewhat quicker than that of the shift-search technique. In this work, in light of the possibility of, an original decreased query table strategy is created to decode the (23, 12, 7) Golay code. The decreased query table utilizing in this calculation comprises of condition designs and comparing error designs which just have one and two errors in the message block of the codeword. The proposed technique fills in as follows: Given a got codeword r, first, the condition s is registered and afterward the heaviness of this disorder w(s) is figured straightforwardly. On the off chance that w(s) =0, it implies no errors occurred in the got codeword. In the event that w(s) $\leqq$3, it implies all things considered three errors occurred in the equality really look at block of the got codeword.

On the off chance that this weight equivalents to 1, it implies there is one error in the equality really look at bit. Along these lines, moving the distinction passed on k bits to frame a 23-bit length word, and afterward the got codeword short (modulo 2) this 23-bit length word and less comparing error example to address the got codeword. For the second and third conditions, the got codeword must cyclic shift left n-k bits, and thusly equality check block and message block are traded, which shows that the errors are additionally traded. Rehashing the techniques over, one can address up to three errors in the got codeword.

The notable twofold inquiry calculation can be utilized to diminish the looking through time, yet the conditions should be masterminded in rising request first. This strategy depends on the way that it utilizes the properties of cyclic codes and the heaviness of disorder to drastically decrease the size of the conventional error example and condition table. Since the parallel Golay code is an ideal code, a weight-4 error happened is constantly decoded as a weight-3 error design by a hard translating technique.

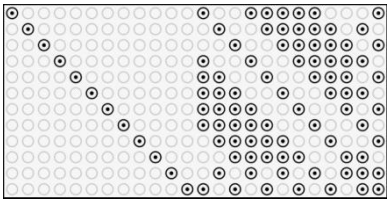

Figure 1.1: Golay Code

The technique proposes utilizing trait vectors to address any kind of information, including yet not restricted to, individual records, vehicle data, and social data set frameworks. The quality vectors are made by noting a bunch of Yes/No inquiries and setting/resetting the grouping of bits appropriately. The proposed procedure additionally endures bit contortion that might happen in the characteristic vectors during the inquiry activity. Our work proposes switching the customary utilization of error correction codes. In error correction codes, a succession of bits that we need to move is changed over to a more drawn out grouping of bits called codeword by adding some additional bits. This codeword is sent over a channel. The recipient site will actually want to recover the first succession regardless of whether the first arrangement (message) has a few bits of error (14) bits relying upon the pre-owned error codes. We consider the disentangling technique as the essential activity, and we expect that a neighborhood of code words might be planned into a more modest assortment of data words. Hash records, which empower looking for double vectors, are to be developed from these information words. The methods proposed in this work will utilize Golay code for error correction and detection. Golay code has two varieties.

1.2 EXISTING SYSTEM

complex directing organization for completely equal engineering intended to deliver the high throughput. Enormous VNUs and CNUs are needed for completely equal engineering. Associations between the hubs depend on the location rationale as opposed to steering organization. The strategy is to plan the somewhat equal based design for LDPC codes and to diminish the directing clog in network. This engineering works on the high throughput. The Golay code was introduced to address error adjusting marvels. The twofold Golay code (G23) is addressed as (23, 12, 7), while the lengthy parallel Golay code (G24) is as (24, 12, 8). The lengthy Golay code has been utilized widely in profound space organization of JPL-NASA just as in the Explorer imaging framework.

Furthermore, Golay code assumes a crucial part in various applications like coded excitation for a laser and ultrasound imaging because of the total side flap invalidation property of integral Golay pair. This load of utilizations need age of Golay arrangement, which is taken care of as trigger to the laser modules. Be that as it may, for creating Golay code a programmed design generator is utilized, which is of extremely significant expense. Broadened Golay Code is otherwise called Golay code (24,

12, 8), where we have codewords of length 24 bits portraying the first 12-bit message.

II. LITERATURE SURVEY

M. Nazeri et al.,[1] The Golay codes are generally utilized Error Correction Codes (ECCs) that are utilized to perceive and address errors in computerized frameworks. This work proposes a productive design for equipment execution of Golay code encoder. The 16 proposed design has three significant units: 1) information unit, 2) control unit and 3) change unit. These units are painstakingly planned to such an extent that the created design can work for a message with '0' and '1' Generally Huge (MS) bits. The exhibition of the created encoder engineering is checked utilizing FPGA gadgets. The outcomes exhibit that the created encoder engineering gives a promising benefit contrasted with other encoder structures for Golay codes.

T. Da et al.,[2] presents centering technique (TFM) draws in much interest due to high picture goal and huge powerful reach. In any case, the sign to commotion proportion (SNR) of TFM is somewhat low because of single-component outflow. Particularly in exceptionally constricting materials, the sign abundancy might be diminished with profundity to a level lower than the electronic commotion presented by the sign procurement framework. Golay-coded excitation was acquainted with conquer this issue, be that as it may, the double-excitations lessen the time goal and may prompt negative deciphering execution because of the overall difference in filtering positions. In this work, the Stomach muscle code transformation factor was utilized to understand the TFM imaging dependent on Golay-coded single-excitation which has a decent presentation as customary Golay-coded excitation. A progression of reenactments and trials were led to look at execution of TFM utilizing un-coded excitation, Golay-coded excitation and changed Golay-coded excitation. TFM utilizing adjusted Golay-coded excitation could beat the hindrances of double-excitation, and has around a similar SNR acquire as TFM utilizing conventional one.

Y. Dong et al.,[3] Stage nonstop and differentiable quadriphase waveforms are coded by the Gaussian least shift keying (GMSK) conspire utilizing Golay double correlative groupings. To fulfill unearthly necessities, the waveforms are additionally enhanced by a range streamlining measure. The extra-low sidelobe level is accomplished by the utilization of expanded bungled channel in beat pressure. To further develop Doppler resistance, the Doppler tough waveforms are determined that give the principal request concealment to the raised sidelobes presented by the Doppler recurrence shift in the bring signal back.

T. Zeng, et al.,[4] present a constant execution of TX/RX DSP for a lucid handset dependent on the lengthy Golay-coded tweak, and work on the affectability by 2.9dB contrasted with PDM-BPSK at a similar bit rate, and propose an incomplete differential technique to take care of the stage uncertainty issue.

M. I. Schope et al.,[5] In this work, waveforms for MIMO staged exhibit radar to upgrade cross-range goal are examined. The issue of high sidelobes in range made by the utilization of Half breed Codes with a single waveform and spatial coding is thought of and a technique to decrease these sidelobes by the utilization of Golay arrangements as spatial codes is proposed. It is shown that the proposed strategy accomplishes a similar reach execution as a staged exhibit radar with one waveform, regardless of making extra sidelobes in Doppler.

P. Zhang et al.,[6] In this work, we propose an equal engineering of the flawed greatest probability disentangling (IMLD) technique, called PIMLD. It is additionally executed onto a FPGA and applied to decode the (24,12,8) expanded Golay code. Test results show that the proposed PIMLD decoder accomplishes 12.0 Gb/s throughput at 500 MHz recurrence. Besides, the idleness for the decoder is just 5 clock cycles.

A. Jose et al.,[7] A productive fast encoding plan of double Golay code (23, 12, 7) alongside its plan and execution in Simple 6 FPGA is introduced in this work. For the proposed encoder, a low dormancy is accomplished by barring straight criticism shift register (LFSR) in the plan. Additionally, a low-intricacy double Golay decoder dependent on disorder disintegration calculation and add-contrast calculation and equal design is proposed which brings about high velocity activity. The proposed design works at a further developed speed when contrasted with the contemporary works distributed around here. A clock recurrence of 344.827 MHz is noticed for the proposed encoder design while the decoder has a speed of 318.471 MHz. For the proposed equipment modules both high throughput and low inertness is accomplished.

T. S. Nidhin et al.,[8] The vulnerability to Single Occasion Upset (SEU) is extremely high for Design memory of SRAM based Field Programmable Door Exhibits (FPGA) contrasted with other FPGA assets. The decrease in highlight sizes and center voltages prompts a decrease in the basic charge needed to change the condition of a memory cell. The SEUs cause disappointments in the framework usefulness carried out in FPGA. Issue lenient strategies must be embraced for reliable application advancement of wellbeing frameworks in FPGAs. The Golay code and the lengthy Golay code shows better error detection and correction capacity than the other error correction codes accessible for SEU moderation in the

arrangement memory of FPGAs. In this work an error recuperation system for setup memory dependent on broadened Golay code has been proposed. Golay encoder module has been executed in Straightforward 6 FPGA and the encoder module runs at 274.122MHz. This work likewise proposes a light test arrangement for approving any of the moderation methods against SEUs in the setup memory of FPGAs.

P. Bhoyar et al.,[9] This work depends on cyclic excess check based encoding plan. High throughput and fast equipment for Golay code encoder and decoder could be valuable in computerized correspondence framework. In this work, another calculation has been proposed for CRC based encoding plan, which without any direct criticism shift registers (LFSR). Likewise, productive structures have been proposed for both Golay encoder and decoder, which outflank the current designs as far as speed and throughput. The proposed design executed in virtex-4 Xilinx power assessor. Albeit the CRC encoder and decoder is instinctive and simple to execute, and to lessen the enormous equipment intricacy required. The proposed strategy it further develop the transmission framework execution level. In this engineering our work is to plan a Golay code dependent on encoder and decoder design utilizing CRC age procedure. This method is utilized to diminish the circuit intricacy for information transmission and gathering measure.

C. Sheelam et al.,[10] This work spreads out two unique methodologies for age of double golay code (23, 12). In particular, Straight criticism shift register (LFSR) based CRC and equipment design dependent on CRC. There are sure detriments related with these two designs. To conquer those hindrances, another design has been proposed for double golay code (23, 12) age. This work additionally presents a proficient equipment design to produce broadened golay code (24, 12). Rapid, low inertness, low region and low force engineering has been planned and confirmed.

III PROBLEM FORMULATION & OBJECTIVE

CRC is assuming a principle part in the systems administration climate to identify the errors. With moving the speed of sending information to synchronize with speed, it is important to speed up CRC age. Most architects know about the cyclic repetition check (CRC). Many realize that it is utilized in correspondence conventions to distinguish bit errors and that it is basically a rest of the modulo-2long division activity. As a fundamental technique for managing information errors normally the equipment execution of CRC calculations depends on the straight criticism shift registers (LFSRs), which handle the information sequentially. The sequential computation of the CRC codes can't accomplish a high throughput.

There is still some of the limitation or challenges in error detecting and correcting code so the observed problem formulation is as followings-

The existing technique based circuit complexity is high for data transmission and reception process. Consume more number of components to design the binary golay code VLSI architecture. The circuit use more latency and consume more power during operate.

3.1 OBJECTIVE

Encoding and decoding is necessary to transmit the data during wireless communication for detection and correction of the errors. There are many of the application over VLSI advance digital signal processing. Golay code is a type of linear error-correcting code used in digital communications. The main objective of the proposed research is a VLSI Implementation of Extended Golay Code for Error Correcting Parallel Decoder FPGA-DSP Applications.

The main contribution of the proposed research work is as followings-

To design a GOLAY code technique based encoder decoder using CRC methodology. This work is to increase the secure level and to optimize the circuit complexity.

Proposed system is to modify the encoder and decoder data bits structure level and to add the message bit, key bit and to apply the these bits into GOLAY binary code technique.

This technique is to apply the majority gate analysis process and to get the final majority output bit and to add the any location in encoder architecture output data bits.

Implementation is performed using Xilinx ISE 14.7 software and check result validation using Isim simulator in test bench window. 4. PROPOSED METHODOLOGY

PROPOSED FLOW CHART

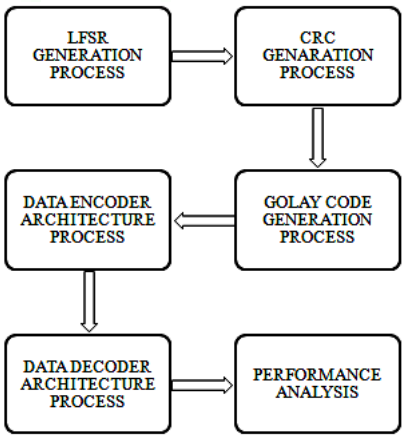

Figure 3.1: Flow Chart

A weight method with using a reduced lookup table is developed to decode the three possible errors in (24, 12, 7) Golay code. The reduced lookup table consists

of syndrome patterns and corresponding error patterns which only have one and two errors occurred in the message block of the received codeword. The useful proposed algorithm.

IV METHODOLOGY

The methodology is based on the followings su module-

- LFSR generation process
- CRC generation process
- GOLAY code generation process
- Data encoder architecture process

This work is to increase the secure level and to optimize the circuit complexity. Proposed system is to modify the encoder and decoder data bits structure level and to add the message bit, key bit and to apply the these bits into GOLAY binary code technique. This technique is to apply the majority gate analysis process and to get the final majority output bit and to add the any location in encoder architecture output data bits. To combat this problem, a hardware module programmed to yield a Golay encoded codeword may be used. Golay decoder is used extensively in communication links for forward error correction. Therefore, a high speed and high throughput hardware for decoder could be useful in communication links for forward error correction.

V RESULT AND ANALYSIS

The implementation of the proposed algorithm is done over Xilinx ISE 14.7. The ISE package processing toolbox helps us to use the functions available in Xilinx Library.

5.1 SIMULATION SOFTWARE

The ISE Design Suite is the Xilinx® design environment, which allows you to take your design from design entry to Xilinx device programming. With specific editions for logic, embedded processor, or Digital Signal Processing (DSP) system designers, the ISE Design Suite provides an environment tailored to meet your specific design needs. Xilinx ISE (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

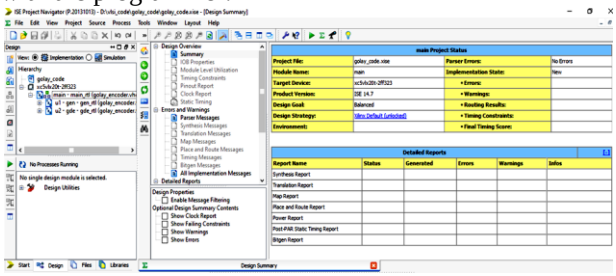

Figure 5.1: Snap shot of Xilinx ISE Design Suite: Logic Edition

The ISE Design Suite: Logic Edition allows you to go from design entry, through implementation and verification, to device programming from within the unified environment of the ISE Project Navigator or from the command line.

5.2 SIMULATION RESULTS AND DISCUSSION

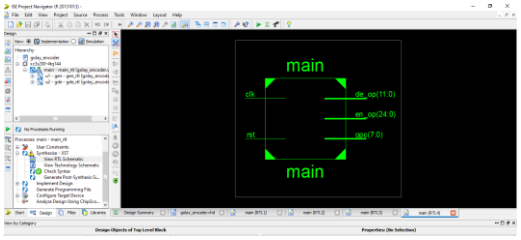

Figure 5.2: RTL View of Top module

Figure 5.2 presents the top level view of the Register transfer level. Initially clock pulse set in logic 1 and applies reset also high using 1. Output shows the 24 bit golay code and 12 bit original message

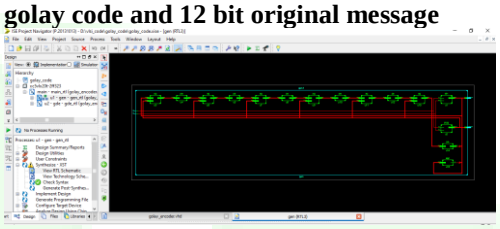

Figure 5.3: RTL on internal block

Figure 5.3 presents the internal RTL view of the proposed golay code circuit. Here red color shows the wire and green colour shows the logic blocks.

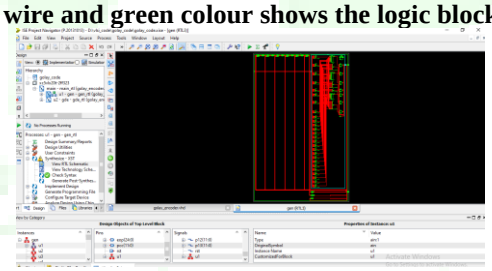

Figure 5.4: Complete RTL View

Figure 5.4 shows the complete RTL view of the golay code. It also shows the technological view as select during the top module processing.

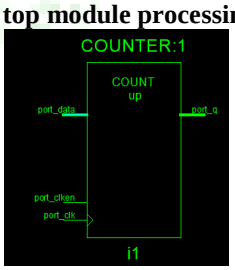

Figure 5.5: Counter

Figure 5.5 is showing the counter design, which is the internal part of the golay circuit. The counter counts the error during transmission. Like golay code (24,12,8) shows the 24 bit of golay code, 12 bit of the message and 8 bit distance to recover the original message or data.

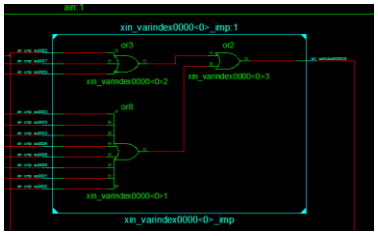

Figure 5.6. Gate symbol

Figure 5.6 presents the GATE logic symbol in the VLSI golay architecture. The AND and OR gate are mostly used in the internal RTL circuit.

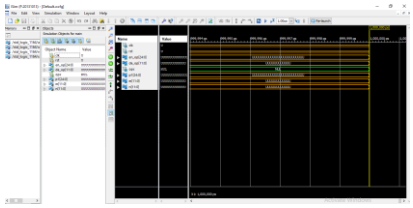

Figure 5.7: High Impedance test bench

Figure 5.7 presents the high impedance of the test bench, to represent the high impedance use symbol Z or U.

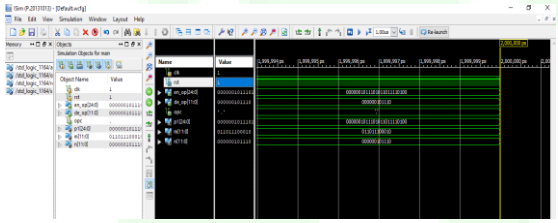

Figure 5.8: Test bench results -1

Figure 5.8 provides the test bench results. Here clock is set at logic 1 or active condition, reset is at 1. Then run the current signal status. The golay code value is 000000101110101011011110100. Data value is 0000000101110. Opc is in null status.

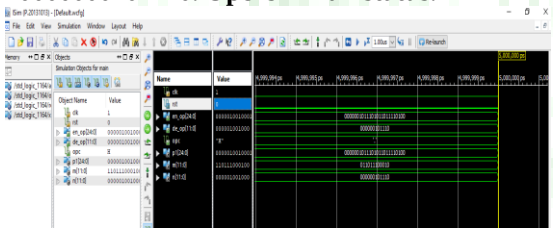

Figure 5.9: Test bench results-2

Figure 5.9 shows the running status of the golay code. The data is starting to retrieve as reset set on the 0 signal. The opc set on the error state and data is retrieving.

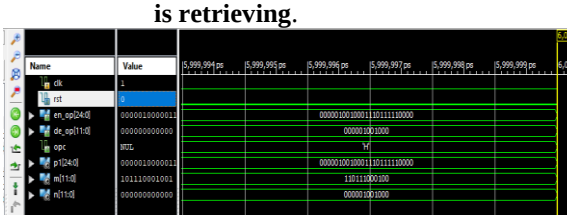

Figure 5.10: Test bench results-3

Table 5.2: Comparison of proposed and previous results

Sr No.	Parameters	Previous Result [1][8]	Proposed Result	Improvement in (%)
1	Methodology	Golay code (24,12,5), (24,12,8)	Golay code (24,12,3) (24,12,6)	NA
2	Area	493	318 (6.6 %)	Aprox 35%
3	Decoder Delay	3.11 ns	1.599ns	Aprox 50%
4	Power	0.76 mw	0.45 mw	Aprox 30%
5	Frequency	NA	625.332 MHz	NA
6	Throughput	NA	7×10^9 or 7GHz	NA

Therefore proposed golay code gives the better performance in terms of the calculated parameters. The proposed golay code optimized the (24,12,3) to (24,12,6) level. The optimized area or component is 318 (6.6 %) while previously it was 493. The delay or latency value is 1.599ns while it was 3.11 ns in existing work. The optimized power is 0.45 mw while previous it is 0.76 mw.

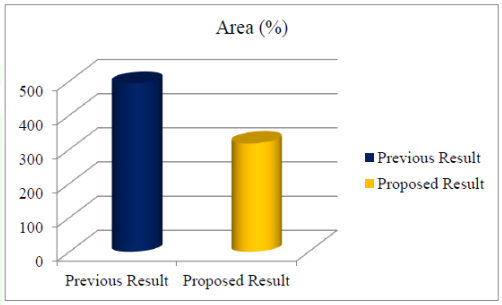

Figure 5.11: Area comparison

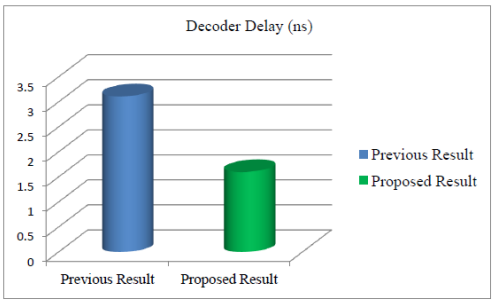

Figure 5.12: Delay comparison

Figure 5.12 is showing the area and delay comparison of the proposed and previous research work. It is clear from the graphical bar chart, proposed golay code scheme gives reduced are and latency or delay.

VI CONCLUSIONS & FUTURE SCOPE

Cyclic Redundancy Check (CRC) is an error-checking code that is widely used in data communication systems and other serial data transmission systems. CRC is based on polynomial manipulations using modulo arithmetic. Finally we design a GOLAY code based encoder and decoder architecture using CRC processing technique. This technique is to reduce the circuit complexity for data transmission and reception process compare to LDPC decoder architecture. Many communication systems use the cyclic redundancy code (CRC) technique for protecting key data fields from transmission errors by enabling both single-bit error

correction and multi-bit error detection. Cyclic redundancy check (CRC) coding is an error-control coding technique for detecting errors that occur when a message is transmitted. Data integrity is imperative for many network protocols, especially data-link layer protocols. Techniques using parity codes and Hamming codes can be used for data verification, but CRC is the preferred and most efficient method used for detecting bit errors produced from medium related noise.

High speed and high throughput hardware for encoder and decoder could be useful in communication field. Due to the channel achieving property, the GOLAY code has become one of the most favorable error-correcting codes. As the GOLAY code achieves the property asymptotically, however, it should be long enough to have a good error-correcting performance. In this project, a new algorithm has been proposed for CRC based encoding scheme, which devoids of any linear feedback shift registers (LFSR).

This research presents VLSI Implementation of Extended Golay Code for Error Correcting Parallel Decoder FPGA-DSP Applications, which outperform the existing architectures in terms of speed and throughput. The proposed architectures were simulated and tested on Virtex-5 platform. Although the CRC encoder and decoder is intuitive and easy to implement, and to reduce the huge hardware complexity required.

The proposed golay code gives the better performance in terms of the calculated parameters. The proposed golay code optimized the (24,12,3) to (24,12,6) level. The optimized area or component is 318 (6.6 %) while previously it was 493. The delay or latency value is 1.599ns while it was 3.11 ns in existing work. The optimized power is 0.45 mw while previous it is 0.76 mw. Proposed technique is to reduce the circuit complexity for data transmission and reception process.

6.1 FUTURE SCOPE

Performance analysis through other new approaches.

- More parameters can be calculated when use different approaches.
- Experiential test in real time environment.
- Implemented multi error correction and detection can be used in real-time IOT based wireless sensor network applications.

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