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Low Power Static RAM Design using Memory Banking for Digital Storage

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***Abstract*— Low-power IC design has been more important in recent years as the number of battery-powered products has grown rapidly. Modern SoCs have a significant number of Embedded SRAM components. When it comes to the new age of rapid mobile computing, traditional SRAM cell designs are power hogs and poor performers. SRAM uses a bi-stable latch circuit to store 1s and 0s. Dynamic RAM (DRAM) must be refreshed to save logic data. SRAM power consumption varies with operating frequency, using more performance at higher frequencies like DRAM. Microprocessor cache requires high-speed memory, hence SRAM may be used. DRAM is used in CPU main memory, where density trumps speed. Industrial, scientific, and automotive electronics use SRAM. This thesis uses memory banking to create a 16-Kb, 1GHz memory in UMC 90 nm technology. The complete design is post-layout simulated and power analyzed. Pre-charge, Row Decoder, Word line driver, Sense amplifier, Column Decoder/MUX, and write driver designs are built to take up the minimal space. The 8 GHz 6T SRAM cell stability is also analyzed. Two adjoining SRAM cells may share a contact, reducing cell layout area. Single cell static, read, and write noise margins are 239 mV, 116 mV, and 426 mV at 1V. Pull-up and cell ratios affect SRAM cell stability.**

Keywords*— Decoder, Analog to Digital Converter (ADC), Static RAM, Dynamic RAM, and Cell stability.

I. INTRODUCTION

It's no secret that battery life is a key issue in the age of rapidly evolving mobile technology and its attendant widespread use. Energy-efficient hardware design is needed when new gadgets like smartwatches, tiny sensor nodes and wireless communication units emerge. Every digital system uses Random Access Memory (RAM) chips, and hence energy-efficient RAM layouts will have a favorable influence on the whole system. In order to keep its contents, a static RAM cell does not need continual reloading. That STATIC RAM is favored over DRAM is due in large part to this particular feature (DRAM). Integrating with CMOS technology allows STATIC RAM to surpass DRAM in terms of System - On - chip (SoC) area consumption (SoCs). Leakage power is becoming a significant source of power consumption as existing technologies scale down to deep submicron levels. Secondly, the STATIC RAM unit houses the vast bulk of the transistors on a device. Because cache memory employs an array design, a single STATIC RAM cell's power decrease may have a significant impact on the total system's power consumption. Because of the simplicity of its construction, the typical 6-transistor (6T) STATIC RAM cell is frequently utilized. The delay and power consumption of the 6T STATIC RAM cell are excellent [1]. A closer look at the traditional 6TSTATIC RAM design reveals that it might use a lot less power [2]. 6T STATIC RAM cells have been the subject of much study in an effort to reduce latency and power consumption so that they may be extensively used in industry. A STATIC RAM array's overall energy consumption may be described as follows: [3]

Etotal = Switching + Leakage

The static energy consumption in the STATIC RAM cell owing to leakage current is represented by Eleakage, whereas ESwitching reflects the energy used in switching activity (learning and composing operations). [4] has examined several STATIC RAM topologies, including 7T and 8T and a new 9T design, however these circuits are more difficult to construct and assure steady operation than

a traditional 6T STATIC RAM cell. STATIC RAM cells with seven transistors (STATIC RAMs) have been reduced in power by using the multi-threshold CMOS (MTCMOS) technology.

Many VLSI devices now incorporate low-power, high-speed STATIC RAMs as a differentiating feature. Particularly in microchips, the on-chip reserve sizes expand with each generation, increasing the gap between processor and cache memory speeds. This is particularly true. STATIC RAM is a cache memory that speeds up the process of assigning processors and memory interfaces. In VLSI innovation, the speed of logic gates has increased, but memory speed has not. As a consequence, high-speed PCs rely on STATIC RAM memories to boost performance, while main memory uses DRAM, where density takes precedence over speed. We aimed to create a high-performance, low-power 6T STATIC RAM for usage in PCs in this research.

The rest of the paper is organized in the following sections section II describes the memory cell and memory banking concepts. In section III we will discuss the design and simulation result of proposed memory element. In section IV we conclude the proposed research and present future work for our research work.

II. THEORY OF MEMORY ELEMENT

RAM is a form of microprocessor chip used to store digital information and program code. RAM is used in PCs, workstations, and servers. Random access lets the PC CPU access any memory directly, rather than sequentially. RAM is near a computer's core and allows quicker data availability than hard discs and SSDs.

a) 6T STATIC RAM

Figure 1 shows a typical 6T transistor, which includes two cross-coupled inverters and two access transistors. STATIC RAM cells are accessed through an access transistor on the output node of each inverter during read cycles. Word line (WL) controls the gate input of the access transistor, allowing access to the STATIC RAM cell. Both reading and writing data from and to the BL or BLB (Bit line) required an accesstransistor control cell..

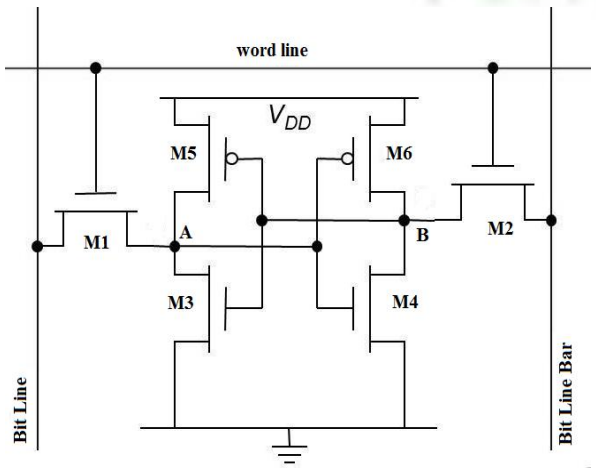

Fig 1. Typical 6T Static Ram Cell

b) Figure A memory bank is a hardware-dependent logical storage facility in electronics that stores data. The memory bank in a computer is determined by the memory controller and the actual configuration of the machine's hardware expansion slots. An SDRAM or DDR SDRAM bank is a collection of rows and columns of storage units that are typically distributed over different chips in the same memory. Because only one bank may be learning and composing at a time, the memory bus's width is specified by the number of bits in each row and column, per bank and chip (single channel). The size of banks is determined by multiplying the number of bits per column and row per chip by the number of chips in a bank. Bank switching is a function that enables computers with many identical RAM banks to switch between them fast. One of the primary distinctions between Harvard-style computers and other kinds of current computers is the presence of two independent sets of memories.

Memory partitioning involves tiling memory arrays and storing the tiles such that maximum data may be given from local memory. Memory banking is used to enhance data transfer and reduce data access conflicts. High-performance circulating memory processors bank dispersed arrays to ensure locality of reference. Memory banking is used in decentralized registrations to minimize communications amongst CPUs. Memory banking divides a huge array into subarrays. Sub arrays, or macros, store sub-word data. The full Word is obtained at once from all subarrays. Slightly elevated STATIC RAM uses 16 macros, but low-power STATIC RAM just needs one.

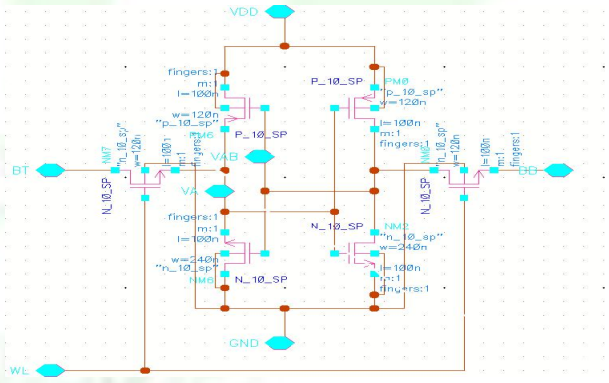

Fig 2. Schematic diagram of 6-T STATIC RAM Cell

III. DESIGN AND SIMULATION RESULTS

In this part we will discuss the propose design of memory cell and the simulation results in term of power consumption, stability analysis and read-write noise margin. The figure 2 illustrates both the design of a 6T-STATIC RAM cell and its symmetrical design structure. The conventional layout features cells that are 7.7125m^2 in size, whereas the cell shown in Figure has just 4.066m^2 of floor space. As a consequence of this, when contrasted with the regular form, the symmetrical construction is capable of saving around 47.21 % of the area required for an arrays of size 3232.

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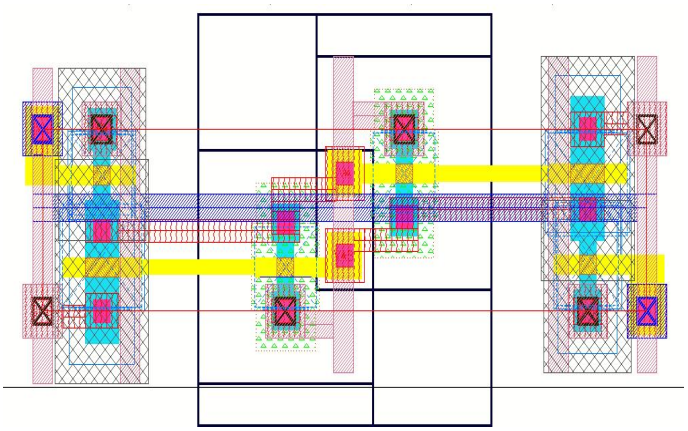

Fig 3. 6-T STATIC RAM Cell with Symmetric Layout.

Now look at the outcomes of running a simulation of a single STATIC RAM cell at a frequency of 8GHz are shown presented in different tables. In order to pre-charge the supply voltage, both bit lines require 20 picoseconds. After then, there is a delay of 25 ps before the write enable signal is activated, and there is another delay of 30 ps before the word line is triggered. In a similar fashion, the sense amplifier is activated when the voltage difference between two-bit lines is 10 percent of the supply voltage. Additionally, the sensor amplifiers required 50 picoseconds to generate single-ended outputs, also known as logic 0 or 1. In conclusion, it is projected that a single operation will take around 125 picoseconds. As a direct consequence of this, the frequencies at which the STATIC RAM Cell operates is 8 GHz. A 16Kb STATIC RAM memory that can function at 1GHz has been built as part of this research by using a banking mechanism.

The Butterfly approach for determining STATIC RAM cell static noise margin (SNM) is implemented here. Static noise margin is used to evaluate memory cell stability under cacophony. The lowest voltage may reverse the storage node state. SNM may be computed using the voltage transfer characteristics of two memory inverters. Memory cell inverter maintains stable states, and their output nodes store data. Storage node noise causes node voltage to change, reducing cell stability. The SNM determines allowable noise reference voltage and inverters' capacity to withstand noise.It may be computed by combining multiple inverter with the largest feasible square, as illustrated in the graphs above, and then computing the cell's SNM as 0.24V for a 1V supply voltage. Cell ratio, pull-up ratio, and power supply affect cell state bit error rate. M3 and M4 driver transistors provide 70% of the noise margin. Cell ratios is driver transistors W/L to access transistor W/L. (M1 or M2).

$$\text{Cell ratio (CR)} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} = \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_2}$$

$$\text{Pull-up ratio (CR)} = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_1} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_2}$$

TABLE 1 Cell Ratio vs. SNM

S.No	CellRatio(CR)	SNM(mV)
1	0.8	231
2	1	236
3	1.5	240
4	1.6	242
5	1.8	248

TABLE 2Pull-up ratio Ratio vs. SNM

S.No	Pull-upRatio(PR)	SNM(mV)
1	0.5	231
2	1	240
3	1.5	248
4	2	251
5	3	255

On the other hand the reading stability parameter. MOS supply voltage and threshold voltage strongly affect it. Cell ratio increases reading noise margin. Pull-up ratio increases the read margin. While determining Read Noise Margin, the design of STATIC RAM inverters is critical. Transistor sizes determine the pull-up ratio. The static and reading noise margin process analyses are comparable. STATIC RAM read noise margin at 1V is 115mV. Likewise write noise margin measures the stability of STATIC RAM Write noise margin affects STATIC RAM cell writing capability. Write margins voltage is the highest bit line noise voltage that supports a write operation. When noise voltage exceeds the write noise margin, the write fails. Noise margin is determined like static noise margin.

TABLE 3 Read noise Margin vs. Cell Ratio

S.No	Read Noise Margin(RNM)	Cell Ratio(CR)
1	104mV	0.8
2	109mV	1
3	115mV	1.5
4	121mV	2
5	125mV	2.4

TABLE 4 Write Noise Margin vs. pull-up ratio

S.No	Write Noise Margin	Pull-up Ratio
1	414mV	0.6
2	419mV	0.8
3	425mV	1
4	431mV	1.2
5	438mV	1.5

IV CONCLUSION AND FUTURE WORK

The proposed designs of this manuscript are organized in different section, first we discuss the the basic theory associated with static RAM in the next section we present the simulation of proposed layout and the results associated with. Here we employed memory banking to produce 16Kb

memory that outperforms monolithic architecture. STATIC RAM has two major paths: read data and row decoder. The general design is changed to postpone the two components. Post-layout simulations and a power analysis have been done. First, a single 6T STATIC RAM cell running at 8GHz is constructed and Process, Voltage, and Temperature (PVT) study is done. A 6T cell having static noise margins of 239 millivolts, 116 millivolts, and 426 millivolts at 1V was produced. While building a cell row and cell array, the design of a single cell is asymmetrical so those cell connections are shared. The cell array's layout area and power dissipation are reduced.

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