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Flash Type Analog to Digital Converter using Dynamic Latch Comparators

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***Abstract*— The existing low power encoder and a latching comparator is suggested for a 4GS/s 5-bit ADC (Flash type). Designing a low-power ADC (Flash type) involves converting temperature code to binary information. The encoder and comparator use dynamic CMOS to decrease ADC (Flash type) power. Using proposed encoder has been developed in 90nm with 1.2V DC. The simulated results of a 5-bit ADC (Flash type) block mainly the latch comparator at 5GHz frequency shows that the Dynamic latch comparators (DLC) outperform the static latch comparator (SLC) and semi-dynamic latch comparator (SDLC) in terms of minimize power consumption and speed of operation. Dynamic latch comparators minimize power, latency, and other issues as well.**

***Keywords*— Decoder,Analog to Digital Converter (ADC), Dynamic Latch comparators (DLC), Static Latch Comparator (SLC) and Semi-Dynamic Latch Comparator (SDLC).**

I. INTRODUCTION

ADC (Flash type) is the quickest ADC. ADC (Flash type) is suited for low-resolution high-speed applications. It's utilized in slightly elevated networks, instrumentation, radar, oscilloscopes, and optical communications. Since ADC (Flash type) uses parallel conversion, gigahertz operation is achievable [1].

Figure 1 shows an ADC flash schematic diagram. ADC (Flash type) design needs 2N-1 comparators for N-bit resolution. An array of comparators compares the input voltage with rising operating voltage. One comparator's analog input is coupled to a single-cycle output. Output of the comparator is in temperature probe code. Encoders convert thermometers codes to binary-weighted output codes. The flash design is fast and can be readily implemented as a series of comparator blocks and an encoder. Exponentially expanding comparators makes it challenging to maintain excellent resolution, broad bandwidth, low power consumption, and compact die size [2].Encoder power is a ADC (Flash type) constraint. Portable devices should merge ADCs with digital circuitry on a single chip. All battery-powered gadgets use low-power approaches to prolong battery life. Because transistor threshold voltages are large, creating a low-voltage ADC is challenging. Low-power ADCs need low-power architecture. For very reduced power requirements, the suggested encoder uses dynamic logic. IT presents background studies.

The rest of the paper is organized in the following sections section II describes the different configuration of flash type analog to digital converter. In section III we will discuss the design and simulation result of proposed ADC (flash type). In section IV we conclude the proposed research and present future work for our research work.

II THEORY OF FLASH TYPE ADC

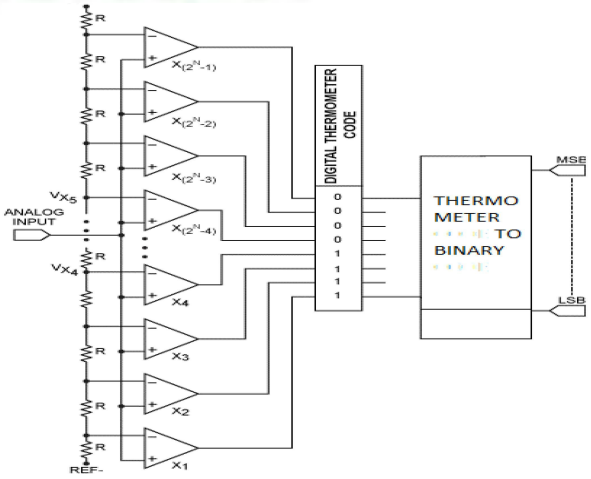

Fig 1. Typical ADC (flash type)

ADCs convert analog stimuli to digital data. Digital signal processing successfully extracts information from signals. ADCs are utilized in telecommunications, acoustic, sensors, video graphy, and more. Low-resolution (4 to 8 bit) ADCs with a fast sample rate are used in oscilloscopes, digital high-speed wireline and wireless connectivity, and radar GHz. High-speed applications use flash and time-interleaved ADCs. First is pipeline ADC. It features a fast shutter speed but a sluggish flash and low resolution. The 2nd ADC is SAR. It's suited for low-power, moderate applications. Third, a sigma-delta ADC. It's ideal for low-speed, high-resolution apps. The 4th ADC is ADC (Flash type). It operates quickly with poor resolution.ADC (Flash type) is the fastest ADC design. ADC (Flash type)s are best for high-speed, low-resolution applications. High-speed instrumentation, radar, digital oscilloscopes, and optical communications employ it. Because ADC (Flash type) employs parallel conversion, it may approach GHz.

5-bit ADC (Flash type) comparator design is equally difficult. Comparator block uses Dynamic Latched Comparator. Static and dynamic flip-flops and locks exist. Unlike a dynamic latch or flip-flop, a static one preserves its content over time. Dynamic latch's output capacitor loses charge over time, causing content loss. Consider using a flexible latch.

A) CMOS Comparator

Dynamic comparators are used in diagnostic and therapeutic applications owing to their latent capacity. It must be Least Significant Bit-precise (LSB). Optimizing comparator energy consumption enhances low-power ADC (Flash type) and IMD battery life. CMOS dynamic comparator was selected for its high-speed, low-power consumption, and high gain. The comparator makes a judgment based on the input signal and reference signal. A single-stage CMOS comparator has been built for speed and low power. This comparator employs back-to-back inverters to convert modest input voltage to full-scale output voltage. Mismatched devices generate an input-referred latch offset, limiting dynamic comparators' precision. Devices also produce kickback noise. Preamplifiers before regenerating latches reduce these difficulties. Preamplifiers amplify input-to-output voltage differences. Boosting preamp gain reduces latch input-referred noise. Comparator inverter buffers isolate the output from heavy loads.

ADCs enable microprocessor-controlled circuits, Arduinos, Raspberry Pi, and other digital logic circuits to engage with the real world. Many digitized systems are integrated with their surroundings by monitoring analogue signals through transducers that sense tone, illumination, temperatures, or movements.

Digital circuits function with binary signals, which have just two distinct states, a logic "1" (HIGH) or a logic "0." (LOW). Analog and digital Converters (A/D) switch between constantly changing analogue and discrete digital signals.

An analog signal converter takes a snapshot of an analogue voltage and outputs a digital output code. A/D converter resolution determines the number of binary digits or bits used to represent analog voltage.

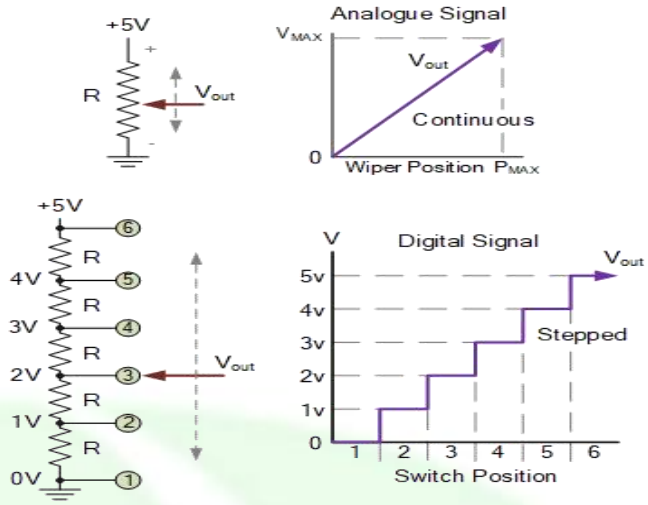

Fig 2. Analog to digital conversion network

B) ADC Characterization

The process of ADC starts with sampling an analogue signal, the conversion speed is determined by the rate at which the input signal is converted to digital form, and the resolution of the ADC is determined by the number of bits produced at the output. The fundamentals of ADC are laid out in this section.

1. **Input Signal Bandwidth**

Bandwidth is the frequency range of an input signal that can pass through analogue front-ended circuitry without amplitude loss. It's the frequency at which a sinusoidal signal's amplitude is reduced by 70%, creating a sinusoidal waveform.

2. Resolution

An ADC's resolution is the smallest amplitude change it can detect. This is the full-scale voltage of the input, not the number of bits used to describe the output digital signal. Precision rises with output bits. A 6-bit ADC separates the incoming signal into 64 levels, offering better precision than a 4-bit ADC. FSR/2N defines the step size, which is the LSB bit voltage, where FSR is the input's full-fledged range.

3. Sample Rate

The sampling process converts analogue sounds to digital. Sample rate, sometimes called sampling frequency, is the number of data signal samples collected each sec. Nyquist theorem, the sampling frequency (Fmax) must be at least as high as or more than twice Fmax to reconstruct a band-limited signal. If the sampling frequency is less than twice the maximum signal frequency, the signal cannot be

correctly reconstructed, and the more instances, the finer the restoration.

4.**Signal to Noise Ratio**

$$SNR=10\log\left(\frac{\text{Psignal}}{\text{Pnoise}}\right)$$

5. Effective Number of Bits

$$\text{ENOB} = \frac{\text{SNR}-1.76}{6.02}$$

6.**Quantization Error**
Quantization error or quantization noise occurs while transforming an analogue signal to digital or digitizing it using a bounded ADC.

7.**Spur- Free Dynamic Range**
SFDR is the ratio of switching frequency amplitude to ADC output spurious signal. SFDR tests ADC quality. Nonlinear ADCs produce false signals, reducing SFDR. Below is the SFDR equation.

SFDR=Signal(dB) -largestspur(dB)

8.**Differentialnon-linearity**
DNL measures the vertical leap gap between the next levels. DNL measures any LSB fluctuation. A perfect ADC outputs 2N uniform voltage levels, each with a fixed width. Ou pas (DNL) is any different from the optimum step width, measured in counts (LSBs).

Optimum ADCs have 0LSB DNL. Building a realistic ADC causes DNL's error. Mismatched DACs may generate DNL inaccuracy in a SAR ADC's mid range. Figure 3.3 depicts the transfer characteristics of a 3-bit ADC. This ADC's input steps should be 1/8 of full-scale (1 LSB of this ADC). Given the ADC's 0V to 8V input range, a 0.5V (Full-scale input range/16 = 0.5 LSB) input change produces the first output-code transition. A 0.5V (Full-scale input range/16 = 0.5 LSB) input change causes the second output-code changeover.

The second transition, from 001 to 010, happens after a 1.25V (1.25 LSB) input shift and is 0.25 LSB too large. The step size changes between levels. Its DNL is 0.75 LSB, indicating the greatest deviation from ideal data transmission step size.

9. Integral on-linearity
Integral nonlinearity is the main difference between actual and ideal finite resolution (INL). INL measures how closely an ADC's output matches its intended response. INL represents the LSB difference between the ADC's actual transfer function and the ideal curve. At each phase, INL is determined by summing all DNL mistakes. INL is derived by plotting the ADC transfer characteristics and identifying the control parameters that deviate the most from optimal outcome.

III DESIGN AND SIMULATION RESULTS

The implementation takes advantage of the dynamic CMOS logic technique. The ADC (Flash type) block consists of three major components:
The dynamic CMOS logic technology is used in the implementation. Each of the three basic components of the ADC (Flash type) block: -

A) Resistor Ladder Block

A resistor ladder divides the reference voltage into 32 distinct levels. A resistor ladder block is seen in Figure 3. The CADENCE Tool's analogue library's 1K resistor.

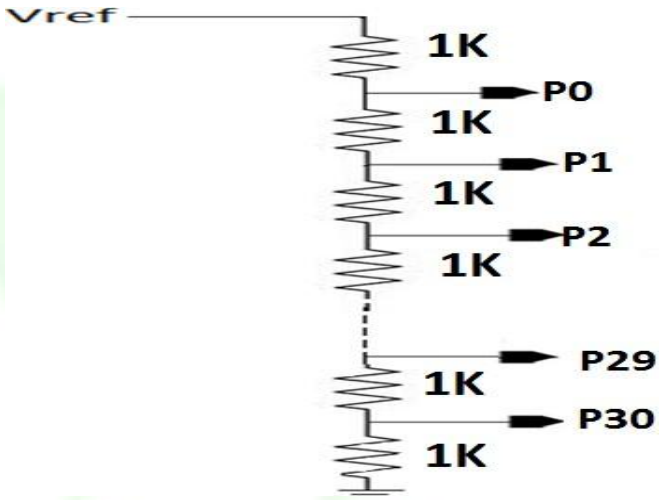

Fig 3. Resistor Ladder Block

It is utilize in the above circuit, a series ladder of 32 resistor of 1K is used in the above ADC (Flash Type).
is utilized in this circuit. A series ladder of 32 1K resistors is used in the ADC (Flash type).

B) Comparator Block

The comparator block consist of preamp circuit, the prime work of the preamp circuit is to boost the small variation in the input signal it can also be termed as pre processor of the input signal the figure 4 shows the schematics and layouts for the preamp. Using a pre-amplifier before the latch may lessen the blow back caused by the latch's regenerating node. As a consequence, the comparator's power usage rises.

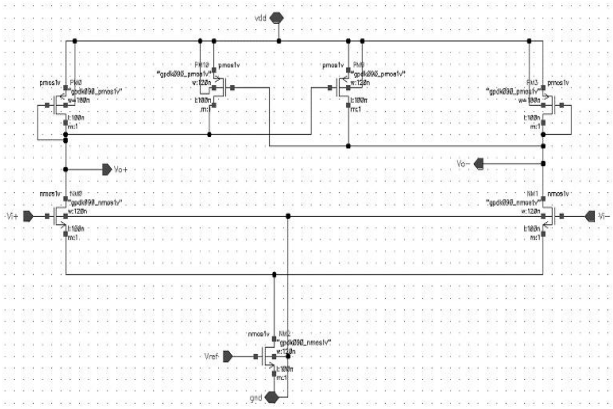

Fig 4. Preamp schematic Block of ADC

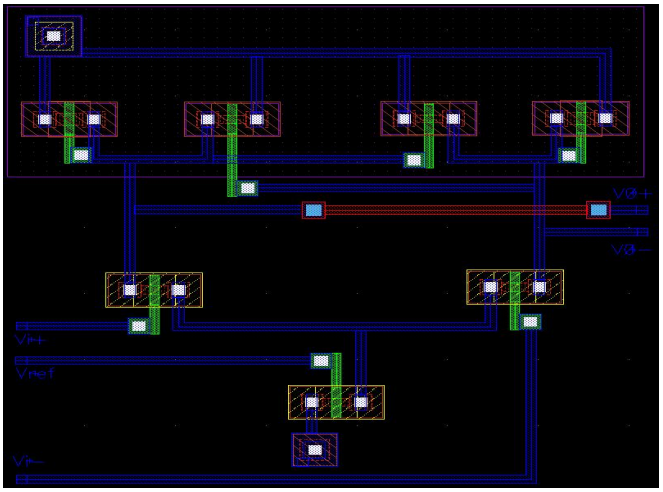

Fig 5. Lay out of comparator block of ADC

C) Dynamic Latch Schematic and Layout

Schematic and architecture of a dynamic latch are shown in the figures 6. A single clock cycle's preamp output value is principally monitored. The clock signal maintains synchronization with the dynamically latch despite its unresponsiveness.

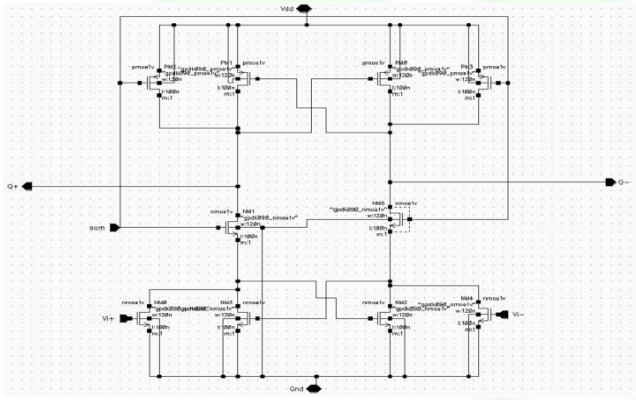

Fig. 6 Dynamic Latch Schematic

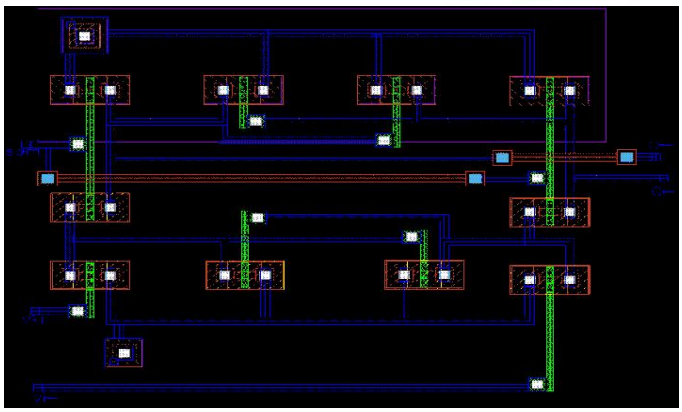

Fig. 7 Dynamic Latch Layout

D) Outputs of ComparatorBlock

The out put of the different blocks are represented in this section figure 8, 9, 10 and 11 shows the DC and transit response of the comparator.

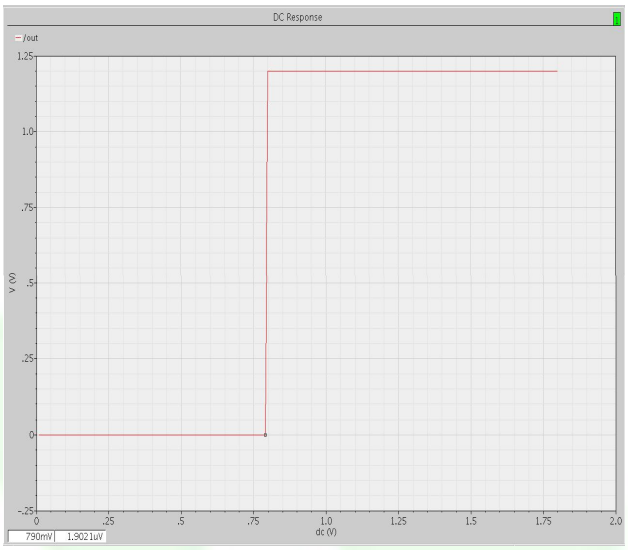

Fig. 8 Voltage Transfer Characteristics (VTC) of the comparator

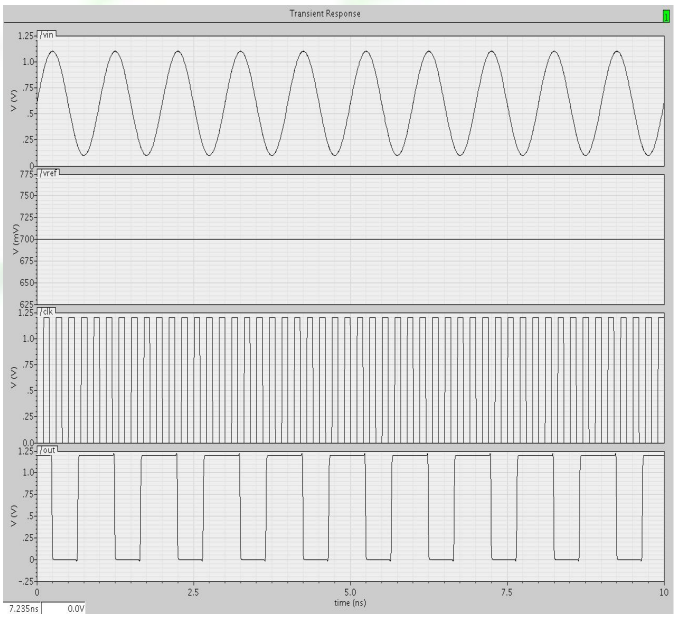

Fig. 9 Transient response of the Comparator (Static Latch)

Fig. 10 Transient response of the Comparator (semi-dynamic Latch)

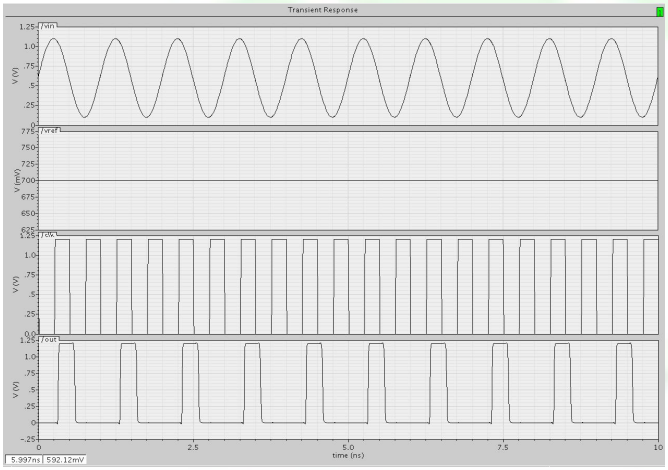

Fig. 11 Transient response of the Comparator (Dynamic Latch)

Table 1. Comparative Table for three Latch Comparator

Performance Parameter	SLC	SDLC	DLC
DC Voltage Supply	1.2V	1.2V	1.2V
Dissipation of Power	135.1µW	73.83µW	69.09µW
Dissipation of Current	112.6µA	61.52µA	57.58µA
Sampling frequency	5GHz	5GHz	5GHz

IV CONCLUSION AND FUTURE WORK

The proposed encoder Encoders are simulated and tested using cadence software on 90 nm technology to observed the performance of different component of ADC (Flash type) the dynamic latch comparator dissipate very less power and extremely fast in operation, the suggested comparator features a high sample frequency to save electricity. The Dynamic latch comparators at 5GHz outperform the static latch comparator and semi-dynamic latch comparator with minimize power consumption. Further research can be done using different w/l technology.

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