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A Review of Literature on Energy Detection Algorithm for WLAN and Wi-Max Applications System

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Abstract* — With the extensive use of power electronics equipment such as rectifier, inverter etc. in power system generates major difficulty related to power quality. One of such difficulties is creation of current and voltage harmonics producing distortion of load waveform, voltage fluctuation, voltage drop, heating of equipment etc. Harmonic current sources, such as computer power supplies, fluorescent lamps with electronic ballasts, elevator drives, and electronic devices using Switch mode power supplies, are commonly found in commercial, institutional, and medical buildings. Active power filters (APF) are the most practical method for harmonic reduction and can be utilized in a variety of situations. In this study, a digital active power filter is used to eliminate harmonics in the source current in a grid system with a non-linear demand. Nonlinear loads are an important component of any power system. With the advent of power electronics, switching elements now account for a significant portion of the electrical load. These constituents cause discontinuities in lines, which increases line losses while lowering power quality as well as sin wave purity. Passive filters are effective in removing harmonics at specific frequencies that are specified in the design. Active filters, on the other side, operate in accordance with the harmonics that are now in play. Active filter designed in this work consists of a shunt active power filter that compensates current harmonic due to non-linear load. The active filter has a voltage source converter (VSC) which works in back to back configuration with a DC coupling capacitor. Power is injected by the VCS at the point of common coupling (PCC). The reference current is generated using instantaneous power theory.

***Keywords*— Sag-Swell, Dynamic Voltage Restorer, Distribution Power System, Voltage Source Inverter, Energy Storage Device, Power System Faults**

I. INTRODUCTION

Wireless communication usage is increasing day by day due to rapid increasing of communication devices. Due to limited spectrum allocation policy, scarcity of spectral resources is increasing while most of the allocated spectrum is underutilized. Most of the useful spectrum is allocated to licensed users that do not utilizes allocation spectrum band in all the geographical locations all the time. The licensed users are those users who paid licensing fee to the government agencies like Telecom Regulatory Authority of India and Federal Communications Commission in the United States. If this unused spectrum is opened for unlicensed user then it becomes promising solution to spectrumscarcity problem. Some of the examples are Wi-Fi and Bluetooth operating in unlicensed bands. These two standards share some part of undesirable spectrum with many other technologies [1, 2].

Cognitive radio has become a promising technology that enables a radio device to monitor, sense, detect electromagnetic radio environment and intelligently adapt its communications channel access in which it exists. CR devices monitor a radio spectrum and modify their operational parameters such as frequency, different modulation schemes, and transmitting power, in order utilize available natural resources. A CR can increase spectrum efficiency leading to higher bandwidth and reduce the burdens of centralized spectrum management by a particular spectrum distribution authority. The cognitive radio is an emerging technology in wireless communication. It is still too early to tell what a cognitive radio seems to be for different wireless applications due to complexity in implementation of cognitive radio in practical.

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II. COGNITIVE RADIO

Cognitive radios "first proposed by Mitola have been chosen as an enabling platform in realizing such dynamic spectrum sharing due to their built-in cognition capabilities. A cognitive radio system is a 'smart' network that can observe the environment, learn from it, and adjust to changing environment conditions. The SAN (software-adaptable network) is analogous to the software-defined radio (SDR) which is the physical control ofthe system that provides the action space for the cognitive process. According to SAN cognitive radio is designed using OODA loop.

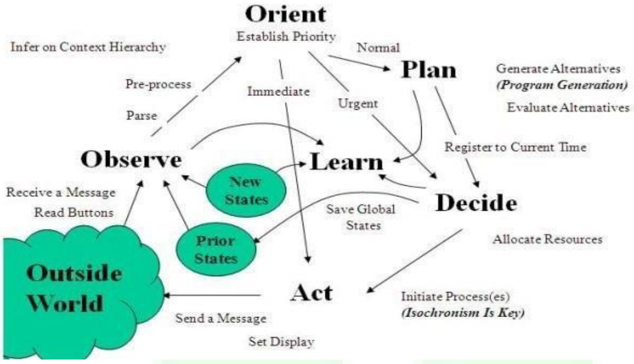

Figure 1: Cognitive radio cycle

The OODA loopis first used for military officers, later on it was adopted for generaldecision making process. The loop consists of four main components with other two components. Cognitive radios first proposed by Mitola have been chosen as an enabling platform in realizing such dynamic spectrum sharing due to their built-in cognition capabilities. A cognitive radio system is a 'smart' network that can observe the environment, learn from it, and adjust to changing environment conditions. The SAN (software-adaptable network) is analogous to the software-defined radio (SDR) which is the physical control ofthe system that provides the action space for the cognitive process. According to SAN cognitive radio is designed using OODA loop. The OODA loopis first used for military officers, later on it was adopted for general decision making process. The loop consists of four main components with other two components:

1. **Observe:** This process senses the network environment and creates an internal model of it. Information can be observed through sensor in SAN or extracted from previous decisions taken from sensed results. Possible information which are directly observed include the presence of spectrum signal from primary and secondary users, received signal-to-interference and noise ratio, packet delays, selection of node parameters location, channel selection ,transmission power.
2. **Orient:** In this process priority are set according to observed information. The cognitive radio elements must interface to sources of networks for effectiveness of cognitive radio to orient it. This step provides guidelines to different cognitive radio elements that how to behave in the network.
3. **Plan:** This schedule are planed according to the systems constraints. This step planned the procedure through which cognitive radio elements work. This process is not good choice.
4. **Decide:** The cognitive process has observed the network environment and is oriented to the end-to-end objectives, it must make a decision. The decision making is a two- step process

a. A centralized decision-making unit that gathers network state data and distributes state information to the nodes of the network, or

b. A distributed process across the network nodes, with each node making decisions under some degree of autonomy.

5. Act: Finally an appropriate action is taken during the act step in which message is send, reconfigure the system and then modify power level.
6. Learn: learning abilities enable communication equipment to evaluate the quality of their past actions. The decision making engine learns from its past successes and failures to tune its parameters and its decision rules to its specific environment.

III. LITERATURE REVIEW

Leelakrishnan, Saranya, 2024, To improve the power consumption, VLSI based power optimization technology is presented in this article. Different elements in WSN, such as sensor nodes, modulation schemes, and package data transmission, influence energy usage. Following a WSN power study, itwas discovered that lowering the energy usage of sensor networks is critical in WSN. In this manuscript, a power optimizationmodel for wireless sensor networks (POM-WSN) is proposed. The proposed system shows how to build and execute a powersaving strategy for WSNs using a customized collaborative unit with parallel processing capabilities on FPGA (Field Programmable Gate Array) and a smart power component. The customizable cooperation unit focuses on applying specialized hardware to customize Operating System speed and transfer it to a soft intel core. This device decreases the OS (Operating System) central processing unit (CPU) overhead associated with installing processor-based IoT (Internet of Things) devices. The smart power unit controls the soft CPU's clock and physical peripherals, putting them in the right state depending on the hardware requirements of the program (tasks) being executed. Furthermore, by taking the command signal from a collaborative custom unit, it is necessary to adjust the amplitude and current. The efficiency and energy usage of the FPGA-based energy saver approach for sensor nodes are compared to the energy usage of processor-based WSN nodes implementations. Using FPGA programmable architecture, the research seeks to build effective power-saving approaches for WSNs **[1].**

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Rohit B. Chaurasiya, 2019, This paper presents implementation friendly VLSI-algorithms for maximum-eigenvalue-detection (MED), energy with minimum-eigenvalue (EME), and mean-to-square extreme-eigenvalue (MSEE) based blind spectrum sensing algorithms. We propose to use efficient iterative power-method for computing maximum and minimum eigenvalues for these algorithms that complemented our hardware design. New VLSI architectures based on suggested spectrum sensing algorithms have been presented in this work. We present two types of sensor architectures: (1) memory-less & low-latency (2) memory-based & resource-shared spectrum-sensor architectures. Former type targets to achieve lower sensing time with adequate hardware efficiency and the later ones are highly resource shared to consume lesser hardware with moderate sensing time. Performance analyses of suggested MED, MSEE and EME spectrum sensing algorithms in AWGN environment showed that the detection probability of 0.75 could be achieved at the SNRs of -12 dB, -10 dB and -7 dB respectively. On synthesizing and post-layout simulating our sensor architectures in 90 nm-CMOS process with the supply of 1.2 V, they could operate at the maximum clock frequency up to 408 MHz delivering sensing time in the range of 23−44 µs. The proposed spectrum sensors have achieved 5.5× and 19× better sensing time and hardware efficiency, respectively, compared to the state-of-the-art implementations. Eventually, the memory-based spectrum sensors are FPGA prototyped and tested, at 100 MHz clock frequency, in DVB-T signal environment with OFDM modulated transmitted signals in 2K size IFFT-mode **[3].**

Heikki Kultala et.al., 2019, This paper proposes a single instruction multiple data (SIMD) processor, which is programmed with high-level OpenCL language. The low-power processor is customized for executing multiple-input-multiple-output (MIMO) detection algorithms at a high performance while consuming very little power making it suitable for software-defined radio (SDR) applications. The novel combination of SIMD operations on a transport programmed multicore datapath allows saving power on both the execution front end and the back end, leading to very good energy efficiency with a compiler programmable design. We demonstrate the feasibility of the architecture with the layered orthogonal lattice detector and minimum mean-squareerror MIMO algorithms, which can be used as a software-defined radio implementation of the 3GPP local thermal equilibrium r11 standard. Compared to other state-of-the-art SDR architectures, the proposed design adds features that improve programmer productivity with an insignificant power and area impact **[4]**.

Antoni Ivanov et. al., 2018, In this article, we proposed an adaptive approach in the spectrum sensing process for improving the performance of existing cyclostationary and energy detectors based on a trade-off between efficiency (sensing time) and accuracy. We introduce adaptivity in the spectrum sensing process as a means to optimize it. We evaluate it in a practical implementation scenario by studying the performance of a cyclostationary detector and an energy detector, both integrated into a framework, which determines the optimal sensing time and was realized in practice through the USRP2 hardware platform. The results we obtain are very close to or better than those from the simulations described in the papers which proposed the implemented spectrum sensing methods. It is also shown that the limited mobility of the SU does not cause a substantial degradation in the performance of the detectors. Therefore, the implementation of these methods in non-stationary devices is feasible. **[5].**

Artem Tkachenko et. al., 2009, The idea of cognitive adios has created a great interest in academic and industrial research. As a result, there are a large number of proposals for their physical and network layer functionalities. However, most of these research results rely on a theoretical analysis or computer simulations. In order to enable this technology and fully understand system design issues in its implementation, these theoretical results should be verified and demonstrated in realistic scenarios through physical implementation and experimental studies. In this paper, we present an experimental platform based on the Berkeley Emulation Engine 2 (BEE2) that can facilitate the development of physical and network layer functionalities for cognitive radios. We take spectrum sensing as an example that incorporates both signal processing and networking techniques to show how this platform could be used to conduct comprehensive research in cognitive radios. In particular, we focus on energy and cyclostationary detectors and indoor network cooperation.The idea of cognitive radios has created a great interest in academic and industrial research. As a result, there are a large number of proposals for their physical and network layer functionalities. However, most of these research results rely on a theoretical analysis or computer simulations. In order to enable this technology and fully understand system design issues in its implementation, these theoretical results should be verified and demonstrated in realistic scenarios through physical implementation and experimental studies. In this paper, we present an experimental platform based on the Berkeley Emulation Engine 2 (BEE2) that can facilitate the development of physical and network layer functionalities for cognitive radios. We take spectrum sensing as an example that incorporates both signal processing and networking techniques to show how this platform could be used to conduct comprehensive research in cognitive radios. In particular, we focus on energy and cyclostationary detectors and indoor network cooperation **[6].**

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Alfonso Troya, Member, 2008, In this paper, we propose low-power designs for the synchronizer and channel estimator units of the Inner Receiver in wireless local area network systems. The objective of the work is the optimization, with respect to power, area, and latency, of both the signal processing algorithms themselves and their implementation. Novel circuit design strategies have been employed to realize optimal hardware and power efficient architectures for the fast Fourier transform, arctangent computation unit, numerically controlled oscillator, and the decimation filters. The use of multiple clock domains and clock gating reduces the power consumption further. These blocks have been integrated into an experimental digital baseband processor for the IEEE 802.11a standard implemented in the 0.25- m 5-metal layer BiCMOS technology from Institute for High Performance Microelectronics **[7]**.

W. Eberle et.al., 2007, With the advent of mobile communications, voice telecommunications became wireless. Future applications, however, target multimedia, messaging, and high-speed internet access, all expressing the need for a broadband high-speed wireless access technique. Both the domestic multimedia and the wireless local area network (WLANs) business markets are addressed. Established systems deliver 2–11 Mb/s based on spectrally inefficient spread-spectrum techniques, where scalability has reached a limit. The next generation of modems requires spectrally more efficient low-power and highly integrated solutions. We describe here the design of two digital baseband orthogonal frequency division multiplex (OFDM) signal processing ASICs, implementing respectively a quaternary phase-shift keying (QPSK)-based 80-Mb/s and a 64 quadrature amplitude modulation (QAM)-based 72-Mb/s digital inner transceiver. The latter partially matches the Hiperlan/2 and IEEE 802.11a standards. Joint development of signal processing algorithms and architectures along with on-chip data transfer, control, and partitioning leads to a low-power, yet flexible and scalable implementation. Both ASICs were designed in a unique object-oriented C++ design flow starting from algorithm level. The ASICs were successfully tested in a 5-GHz testbed both for file data transfer and web-cam multimedia transmission **[8].**

Nachiketh R. Potlapally et.al., 2006, Security is becoming an everyday concern for a wide range of electronic systems that manipulate, communicate, and store sensitive data. An important and emerging category of such electronic systems are battery-powered mobile appliances, such as personal digital assistants (PDAs) and cell phones, which are severely constrained in the resources they possess, namely, processor, battery, and memory. This work focuses on one important constraint of such devices—battery life—and examines how it is impacted by the use of various security mechanisms. In this paper, we first present a comprehensive analysis of the energy requirements of a wide range of cryptographic algorithms that form the building blocks of security mechanisms such as security protocols. We then study the energy consumption requirements of the most popular transport-layer security protocol: Secure Sockets Layer (SSL). We investigate the impact of various parameters at the protocol level (such as cipher suites, authentication mechanisms, and transaction sizes, etc.) and the cryptographic algorithm level (cipher modes, strength) on the overall energy consumption for secure data transactions. To our knowledge, this is the first comprehensive analysis of the energy requirements of SSL. For our studies, we have developed a measurement-based experimental testbed that consists of an iPAQ PDA connected to a wireless local area network (LAN) and running Linux, a PC-based data acquisition system for real-time current measurement, the OpenSSL implementation of the SSL protocol, and parameterizable SSL client and server test programs. Based on our results, we also discuss various opportunities for realizing energy-efficient implementations of security protocols. We believe such investigations to be an important first step toward addressing the challenges of energy-efficient security for battery-constrained systems **[9].**

Jerome Peter Lynch et.al., 2004, A low-cost wireless sensing unit is designed and fabricated for deployment as the building block of wireless structural health monitoring systems. Finite operational lives of portable power supplies, such as batteries, necessitate optimization of the wireless sensing unit design to attain overall energy efficiency. This is in conflict with the need for wireless radios that have far-reaching communication ranges that require significant amounts of power. As a result, a penalty is incurred by transmitting raw time-history records using scarce system resources such as battery power and bandwidth. Alternatively, a computational core that can accommodate local processing of data is designed and implemented in the wireless sensing unit. The role of the computational core is to perform interrogation tasks of collected raw time-history data and to transmit via the wireless channel the analysis results rather than time-history records. To illustrate the ability of the computational core to execute such embedded engineering analyses, a two-tiered time-series damage detection algorithm is implemented as an example. Using a lumped-mass laboratory structure, local execution of the embedded damage detection method is shown to save energy by avoiding utilization of the wireless channel to transmit raw time-history data **[10].**

III. VLSI Implementation of Energy Detector Technique

A. Pseudo Random Generator - The sequence generated by PRSG. It is a shift register whose input is taken as random value. The only single bit is function of XOR logic. Here first input bit provided by taking linear XOR function of first and last bit. The other bits are depended on

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previous bit. The operation is deterministic to generate random bits. The sequence of bits are produced by shift registers and its current state completely determined by its previous state. The register has finite number of states and random sequence is repeated after some cycles. The PRSG can be well explained in Figure 4-2. It produces a sequence of bits which is random and generates a long
cycle sequence. [20]

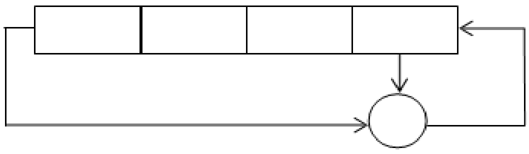

Figure: 2: XOR operation of Pseudo Random Sequence Generator

B. Data Generation Using Pseudo Random Sequence Generator- The random sequence generator has generated by using Pseudo-random-Sequence- Generator (PRSG). The PRSG is constituted from four registers and total number of sequence generated is=24-1. The detail about random sequence generator is explained in previous chapters. The generator of random sequence is little bit different than the previous sections. In this part random sequence is generated by XORing output of LSB and output of MSB. The block diagram is shown in Figure 4-5
.

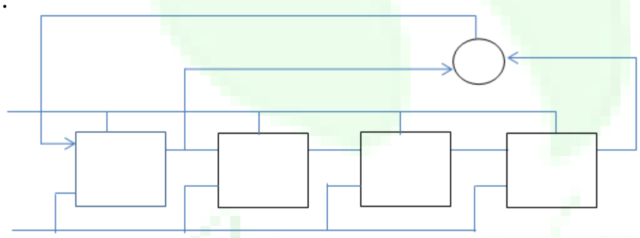

Figure :3 Block Diagram for Pseudo-random data generator for BPSK Modulator

The PRSG responds to positive edge triggered of clock signal and negative edge triggered reset signal which forces the register to logic 1 level. The rising edge of clock makes the data of DFF transferred to its output Q.

C. VHDL implementation of OFDM for Energy Detection - The OFDM modulation is a multicarrier modulation. The single carrier modulation using VHDL is designed in previous section. The basic blocks to design OFDM is signal mapper to implement BPSK modulator, serial to parallel converter, IFFT block, parallel to serial converter and then energy detector. This chapter frame out the entire module to implement OFDM [21].

V. CONCLUSION AND FUTURE SCOPE

The To conclude this review, the integration of the OODA loop into cognitive radio systems demonstrates a promising framework for advancing dynamic spectrum sharing through intelligent, adaptive processes. This synergy enables cognitive radios to respond effectively to changing environments by observing, orienting, deciding, and acting, while continuously learning from past experiences.

The literature reviewed highlights the diverse advancements in wireless communication, emphasizing the importance of energy efficiency, hardware optimization, and spectrum sensing in achieving robust and sustainable cognitive radio systems. From VLSI-based solutions to IoT-integrated frameworks and spectrum sensing methodologies, these innovations collectively shape the future of wireless networks.

Through experimental and theoretical approaches, researchers have outlined the challenges and opportunities in deploying cognitive radios, especially in scenarios requiring real-time decision-making and adaptive functionalities. These findings underline the critical role of implementing efficient hardware designs and robust algorithms in optimizing the performance and energy usage of next-generation wireless systems.

In essence, the adoption of the OODA loop, coupled with ongoing innovations, is poised to transform cognitive radio systems into highly efficient and intelligent networks, paving the way for advanced applications in dynamic spectrum management and beyond.

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