A Review Paper on Second Generation Current Conveyors

Vijay[1], Dr. Rinkesh Mittal[2]
Student M.Tech VLSI[1], Professor[2]
[1]Department of Electronic and Communication Engineering
Chandigarh Engineering College, Landran, Punjab, India
[1]vj.rana0001@gmail.com
[2]hod.coeece@cgc.edu.in

Abstract: **In the modern day analog circuit design, current conveyors are widely used than Op-amps, due to its optimized characteristics like low power, low voltage, higher slew rate, compactness. In this paper, the CMOS current conveyor design approaches, used by various researchers have been reviewed. The researchers have proposed enhanced current conveyor design and compare their results with existing approaches. Many designers have presented the optimized current conveyor circuits as compared to existing results. Two types of topologies i.e. Translinear loop and Differential loop are used by designers to design current conveyors. This paper discusses many parameters like static and dynamic behaviour improvement, electronically tuned current conveyors, novel current conveyors, Meta heuristic techniques etc. mentioned by researchers. These current conveyors are used to design multifunction filters, oscillators, integrators, differentiators, radio frequency designs etc. The researchers have improved the linearity, compactness, Q-factor, series resistance, programmable gain and bandwidth**.

Keywords: **Current mode, Second generation current conveyor, Low voltage, Low power, voltage swing.**

I. INTRODUCTION

Due to the technology advancements in analog circuit design, the size of the transistors is reducing, which leads to the more mixed mode integrated circuits. Analog active devices are widely used in battery operated portable devices such as laptops, mobile phones, bio-implantable devices and in numerous other applications.[1] In early times, analog designers use voltage mode operation in which voltage signals are applied through nodes. We use a building block such as Op-amp to add, subtract, attenuate, and amplify and filtrations of voltage signals [2]. It works on low power, low voltage but it has some drawbacks like small slew rate, smaller bandwidth and diminishing voltage swing.

Because of the technology scaling, the focus of industry and academia goes towards low voltage (LV), low power (LP), and current mode (CM) analog circuits [2]. CM circuits has been emerges as precise, low voltage, low power operation, high slew rate, large bandwidth, low voltage sensitivity and large signal processing [3]. CM circuits have local nodes in which current signal is flows through branches rather than nodes as in voltage mode circuits. It has both low impedance node and high impedance node to make design more convenient. Several CM devices are available such as current conveyors and current feedback operational amplifiers. As compared to Op-amp, these have constant bandwidth, high slew rate and higher frequency operations. Thus CM circuits have more importance in designing of LV, LP integrated circuits [2]. In CM circuits, current conveyors (CC) are best suited for wide bandwidth applications. CC is nothing but a basic building block for current mode circuits. CC is a three terminal device, which conveys the current between two different impedances levels [4].

The evolution of the CC begins, when A.Sedra and K.C.Smith suggested 1st generation CCI. After that CCs becomes need of the hour and widely adopted by analog designers as a building block of analog circuits [5], it replaces Op-amp in analog circuits design. Two years later, A.Sedra and K.C.Smith presented the second generation CCII which enables wide range of application [6] such as analog filters, oscillators, signal processing. At the beginning the CCII is proposed for BJT technology , which results in good current and voltage bandwidth performance, but later we uses MOS technology to achieve higher gain, bandwidth and higher slew rates[7]. CCII has one high and low input port impedances respectively as compared to CCI which has two low impedances.

Researchers have demonstrated CCs into three categories- CCI, CCII, and CCIII. These all circuits have similar structures but they posses different characteristics. CCs consists of three ports named as x, y, z. It utilizes x, z terminals as current follower and y, x terminals as voltage follower. Current from terminal x is mirrored through z.

First generation Current conveyor (CCI) was presented in 1968 by A.Sedra and K.C.Smith [4]. it has three terminals x, y, z. Potentials at terminals y and x are equal, so that equal current flows across terminals x and y, which is conveyed through

terminal z. CCI has two types of operations, (CCI+) and (CCI-). In (CCI+) current through x is mirrored to z and in (CCI-) current through port x is flowing out of z. The block diagram and impedance levels of CCI are as shown below:

CCI Ports	Impedance Level
Port X	Low (ideally zero)
Port Y	Low (ideally zero)
Port Z	High (ideally infinite)

Table-Impedance level at different ports of CCI

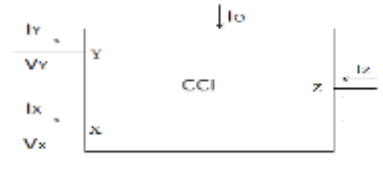

Figure-Block Diagram of CCI

Two years later, 2nd generation current conveyors (CCI) are presented by A.Sedra and K.C.Smith as an advancement of CCI, which have capabilities of using high impedance levels and reduced loading effect. It employs two different impedance levels as compared to CCI. The current through node y=0, and current will be conveyed to high impedance terminal z. CCII has unity gain, wide bandwidth characteristics. The block diagram and impedance levels of CCII are as shown below:

CCII Ports	Impedance Level
Port X	Low (ideally zero)
Port Y	High (ideally infinite)
Port Z	High (ideally infinite)

Table-Impedance level at different ports of CCII

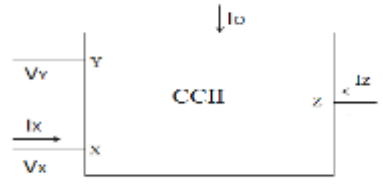

Figure-Block Diagram of CCII

CCII has increased gain bandwidth product and slew rate, also used as an applications in differentiators, integrators, multifunction filters.

In 1995, Fabre proposed the third generation CCIII [8], similar to CCI but currents on x and y flows in opposite direction. It has unity gain and can be used as current measurement and acts as current controlled current source. It has high linearity, wide frequency response, accuracy. CCIII are widely used in multifunction filters. The block diagram of CCIII is as shown below:

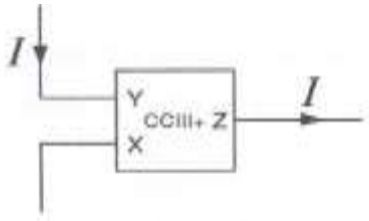

Figure-Block Diagram of CCIII

II. LITERATURE REVIEW

Antonio J. Lopez-Maetin et al. [1] design a bi-quadratic filter using FVF technique with CC. This circuit uses LP and operates at 1.5V power supply. It has simple circuitry and enhanced bandwidth up to 100 MHz's. The proposed circuit is simulated using 0.5um CMOS technology.

A Flipped voltage follower (FVF) based CCII design is suggested by **Amisha.P.Niak and Niranjan.M.Devasharyee** [2]. It uses Class A topology to obtain gain of almost unity and bandwidth upto 100 MHz. This circuit uses 0.5um CMOS technology and consumes less power. The proposed circuit is compact and uses only 10 transistors.

Manish Tikyani and Rishikesh Pandey [5] suggested a LV CM design. It comprises of 4 pmos and 5 nmos transistors, that are operates at 1.3V power supply Wide frequency range is achieved by using compensating technique. Bandwidth is increased from 60 MHz to 163 MHz by using resistive compensation method. The proposed circuit is simulated using Cadence design in 0.18um Technology.

Samir Ben Salem et al. [6] presented the improvised CCII in translinear cmos design by improving static and dynamic behaviour. This CCII is further designed for RF design, in which voltage mode Band pass filter and tunable current forms a basic building block. This design is operated at low supply voltage of 2.5v and the DC biasing is done to improve series resistance Rx. The electronically tuned band pass filter with high Q-factor (88-313) is simulated using PSPICE simulation.

A low power electronically tunable CCII (ECCII) is suggested by **Shu-xiang song et al.** [9] which is based on Translinear loop circuit. Current transfer characteristics have been obtained by dc biasing. This proposed ECCII operates at 1.2v power supply, which results in LP dissipation. High linearity and programmable current gain is achieved and the new design is simulated using

HSPICE (LEVEL=49) simulation. This design uses TMSC 0.35um CMOS technology.

Yan-huixi and Li Liu [10] presented a Novel CCII to design active filters in CMOS Translinear design. This design has simple circuitry due to less number of active and passive elements. It utilizes the intrinsic property of proposed Novel CCII. Biasing is done at 5uA current and 2.5v power supply. The proposed circuit is electronically adjustable and efficiently used in IC technology.

Moontree kumngern and Soymot Junnapia [11] presents sinusoidal oscillator as an application of single element CCII in Translinear mode. Integrated circuits are implemented by biasing the CCII and oscillator parameters are electronically adjustable and less sensitive to active and passive elements. The proposed circuit is simulated in PSPICE at 1.5v power supply.

Norathadpong Meechuea, Boonruk Chipipop et al. [12] suggests a high frequency model of (CCII-) based on translinear loop. It's transfer function is find using MATLAB programming by comparing Fabre's outside-in and equivalent circuit modelling. The proposed circuit is simulated at 1.2v power supply using RF BSIM4 Level 54 model

Nadhmia Bouaziz Ell feki and Dorra Sellami Masmoudi [13] realizes radio frequency active filters in CM by using CCII and CCIII. The proposed circuit is operated at 2.5V power supply and uses translinear configuration. The central frequency and cut-off frequency of filters is increased. PSPICE simulation is done by using 0.35um technology to obtain theoretical analysed results.

Wang Chunhua, She Zhixing et al. [14] proposed a 0.5 um CMOS CCII using Translinear and CM technique. The circuit is easily realised in fabrication and widely applicable. A simple, LP and high impedance CCII is obtained by simulated the proposed circuit.

An optimized CC is suggested by **A.Sallem et al.** [15] based on Meta Heuristics technique. He uses various algorithms such as Genetic Algorithm (GA), Simulated Annealing (SA) and Particle Swarm Optimization (PSO). These Meta Heuristics algorithms are implemented to obtain highly efficient CCII. CMOS Transistor sizing is done to achieve good performance. This technique is simulated in SPICE using MATLAB software.

A rail to rail, TMSC 0.18um LVDCC circuit based on Differential circuit design is proposed by **Sanjay K.K et al.** [16] for low voltage applications. A LV CM design is used with current amplifiers to optimized the gain. The rail to rail output voltage swing ranges from -1.3V to 1.4V. This circuit posses high linearity up to 90% with unity current gain. The proposed circuit is verified using SPICE simulation.

Montree Kumngern [17] presented a 0.5um MIETEC, Differential difference CC (DDCC) having variable current gains. Log –antilog current amplifiers are used for linear current circulation. These amplifiers consist of one DDCC and four MOS diodes. PSPICE simulation is done at 2.5V supply to obtain adjustable gain.

A Differential pair, LV, LP Oscillator is suggested by **Jitendra Jain, Shobhit Singh et al.** [18]. This circuit is based on differential pair topology. The proposed circuit is design to have high accuracy and wider bandwidth. This design uses 14 transistors, 0.70V power supply. It is simulated on 180nm CMOS technology.

A quadratic oscillator is proposed by **Boonying Knobnob** [19] using CM design. It consists of two grounded capacitors and Translinear CCCIIs respectively. The proposed circuitry is simple and has less power dissipation. The CCCIIs are biased is done in order to control Oscillator frequency and phase difference. PSPICE simulation is done to verify the proposed circuit.

A CM universal filter having three inputs and single output is suggested by **Montree Kumngern and Jirasak Chanwutitumet al.** [20]. This electronically tunable circuit is used for realization of analog filters. Quality factor and natural angular frequency is adjusted by biasing. Due to simple circuitry, it is used in IC technology.

III. CONCLUSION

In this paper, various topologies to design current conveyor are discussed. The translinear loop based design topology is efficient for high frequency applications; while differential loop based design topology is better for low voltage operations. By taking an idea from these topologies, we can design an efficient current conveyor for low voltage, low power, variable gain and radio frequency applications.

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