Design of Low Voltage Low Power Operational Amplifier

Lakshmi Sunanda. Chikkala[1], N.G.N Prasad[2], D.Mahesh Varma[3]

[1]P.G Student, Kakinada Institute of Engineering and technology, korangi, JNTUK , A.P, INDIA
[2]Assistant professor, Kakinada Institute of Engineering and technology, korangi, JNTUK ,A.P, INDIA
[3] Assistant professor, Kakinada institute of engineering and technology, korangi, JNTUK ,A.P, INDIA
[1] ch.sunanda02@gmail.com,[2]prasad471@gmail.com,[3]maheshvarma@gmail.com

Abstract— **With the demand of low power applications, running circuits with reduced supply voltage can be of great advantage. Integrated circuit designers start to face a power wall as the most difficult constraints in new technology and circuit development are not triggered by process scaling factors, but by barriers imposed by packaging and cooling. The demand of circuits with reduced power consumption and the very fast growing market of portable electronic equipment are increasing the interest in very low power integrated circuits.**

In order to maintain the required performance, lowering the supply voltages implies decreasing transistor's threshold voltages, which brings about a series of problems both in technology and circuit design. The margin for error becomes so small, that any uncertainty in device or circuit parameters may dramatically degrade the performance of actual fabricated chips. As circuit design relies crucially on simulations, the only possibility to overcome these problems is to use highly precise tools to simulate both the fabrication process and the circuit behavior.

Realizing that the conventional circuit design tools can not be used much longer to accurately predict circuit behavior an integrated simulation environment where all efforts to achieve maximum accuracy are taken into account. It links together Tanner tools with the accurate simulators. Active devices are characterized with device simulators and a table-based circuit simulator is used to avoid errors introduced by the fitting parameters procedures in compact models. In this work a technology suited for 0.5 V power supply is developed, and several very low power digital and analog circuits.

Keywords— **Op Amp, CMOS,LVLP ,Nanometers ,FinFet.**

1.INTRODUCTION

Need for Low Voltage Low Power Circuits

There are many factors that are driving the need to have lower power supply voltages in CMOS integrated circuits. As the channel lengths of CMOS technology decrease, the maximum allowable voltage will decrease. Also, as more components are included in the same area on integrated circuits, the power dissipation increases. Finally, the requirement for portable electronics implies battery operation which favors low voltage and low power circuits. These factors and others have caused many to suggest that future implementation of mixed analog digital circuits using standard CMOS will have power supplies of 1.5V or less an important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not anticipated to decrease much below what is available today. It is necessary that the analog power supply be at least equal to the sum of the magnitudes of the n-channel and p-channel thresholds. This implies that low voltage analog circuits are incompatible with the CMOS technology trends of the future. Ways to circumvent this conflict are to develop technologies with lower thresholds, increase the lower voltage power supply by on-chip dc-dc converter, or develop circuit techniques that are compatible with future standard CMOS technology.

Low voltage circuits are needed because:

1. As the device channel length is scaled down into sub- microns and the gate oxide thickness becomes only several nano meters thick, the supply voltage has to be reduced in order to ensure device reliability. With deep submicron processes and FinFet process now available, the maximum allowable supply voltage is decreasing from 5V to 3V and even to 1.5V.

2. The increasing density of the components on chip dictates low power. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating.

3. Portable, battery-powered equipment needs low power to ensure an acceptable operation period from a battery, and the supply voltage must be as low as possible to reduce the number of batteries used.

Low voltage Low Power Techniques in Analog Circuit Design

1. Technology Consideration

Threshold voltage is not proportionally reduced for scaled down technologies. A natural solution is the use of multi-threshold process technologies. Unfortunately, this kind of technology is more expensive and frequently not easy to reproduce. Multi-threshold process technology is expensive due to fabrication process. Higher fabrication cost presents for a multiple-v_{th} technology also suffers from reliability problems. Some design advantage can be obtained by using BICMOS technology at the expense of additional cost, since more fabrication steps are involved. It has been the care that designers using BICMOS technology produce circuits with better performance than CMOS based deigns.

2. Transistor model capable to provide performance and power tradeoff

. For CMOS analog circuits, when the transistors weak inversion region, *gm/ID* reaches the maximum, hence the minimum power consumption can be achieved due to the small quiescent current at the expense of large silicon area and slow speed. When MOS transistors operate in strong inversion, however, although good frequency response and small area are obtained, non-optimum larger power is consumed, and V_{DS} (*sat*) is high. For most analog circuits, the best tradeoff among area, power and speed can be achieved when the transistors work in moderate inversion region but conventional MOS transistor models provide different sets of equations for weak and strong inversion regions, even in computer simulation tools.

MOSFET	CURRENT	VGS,VDS	W	L
MB1	1μA	0.95V,0.95V	12.2μ	10μ
MB2	1Ma	0.95V,1V	12.2μ	10μ
MB3	1μA	0.95V,0.8V	12.2μ	9.95μ
MB4	1Ma	1V,1V	5.35μ	10μ
M8,M9	1Ma	1.2V,1.2V	3.4μ	15.15μ

If this current goes to zero then, this requires a delay in turning the mirror back on because of the parasitic capacitances that must be charged. For example if V_{id} the differential voltage is large enough to turn M1 on and M2 off. Then all of the I(M5) flows through the M1 and none through M2, resulting in I(M5)=I(M1) and I(M2)=0. If I(M3) and (M4) are not greater than I(M5) then the current through M8 will be zero. To avoid this we have to take I(M3) and I(M4) normally between I(M5) and 2I(M5). In the current design this is I(M3)=I(M4)=1.5 times the I(M5).

2 .OP-AMP PRACTICAL CONSIDERATIONS

1. Input/Output Offset Voltage

Op-amps do not always perform practically as they should theoretically. For example, sometimes an output voltage exists when both inputs are grounded. This output voltage is called output offset voltage and it is caused by an input offset voltage. If one is known the other can be calculated,

$$V_{io} = \frac{V_{oo}}{A_v}$$

Imperfect transistors contained in the differential amplifier are responsible for the input

offset voltage, which is usually no more than 2mV. The offset null pins on the IC op-amp can be used with a potentiometer to take care of Vio and Voo.

2. Input Bias Current / Input Offset Current

Similar to the offset voltages, there are currents flowing in or out of the inputs, and their average is known as input bias current, which may have a value of 80nA+. The currents on each input are not always equal and the difference between them is the input offset current. This is important because if the input bias currents are different, then the output voltage can be affected. So to keep the currents the same, each input needs to see the same resistance to ground, since identical currents will flow through identical resistances.

3. Common Mode Rejection Ratio (CMRR)

The common mode rejection ratio (CMRR) is a ratio of the normal high gain that amplifies the difference of the signals on the inputs to the undesirable gain that amplifies a value when the signals are the same.

$$CMRR = A_{diff}/A_{cm}$$

If op-amps were perfect, then there would be zero amplification when the same signal, or common-mode signal, feeds each input. The common-mode signal may be noise, so obviously it is not a good thing to amplify this noise. An acceptable CMRR is in the 90's (dB), where

$$CMRR = 20 \log (A_{diff}/A_{cm}) \quad \{\text{in decibels (dB)}\}$$

4.Output Short-Circuit Current

Op-amps do not output unlimited current because too much current flow could be damaging to the op-amp, particularly if a short circuit develops. Op-amps are made this way on purpose. An output short-circuit current of 25mA is a common value for an opamp. It follows that a low resistance load does not drop the expected voltage.

3.SIMULATION AND RESULTS

In designing a LVLP Opamp, the designers starts with building blocks whose performance can be analyzed to a first order approximation by hand/calculator methods of analysis. The advantage of this step is the insight it provides to the designers as the design of the circuit develops. However, at the some point the designer must turn to a better means of simulation. For the CMOS Opamp this is generally a computer-analysis program such as HSPICE. With the insight of the first order analysis and the modeling capability of HSPICE, the circuit design can be optimized and many other such as tolerance, stability and noise can be examined.

Fabrication allows the simulation and layout of the MOS Opamp. After fabrication the MOS Opamp must be tested and evaluated. The techniques for testing various parameters of the Opamp can be complex as the design of the Opamp itself. Each specification must be verified over a large number of opamps to ensure a working Opamp in case of process variations.

The Objective of this section is to provide the background for simulating and testing a LVLP Opamp. Consider the methods of simulating an Opamp that are appropriate to HSPICE but the concepts are applicable to other types of computer simulation programs. because the simulation & measurements of the amplifier are almost identical, they are presented simultaneously. The only differences found is in parasitic that are actual measurement introduce in the Opamp circuit and the limited bandwidths of the instrumentation.

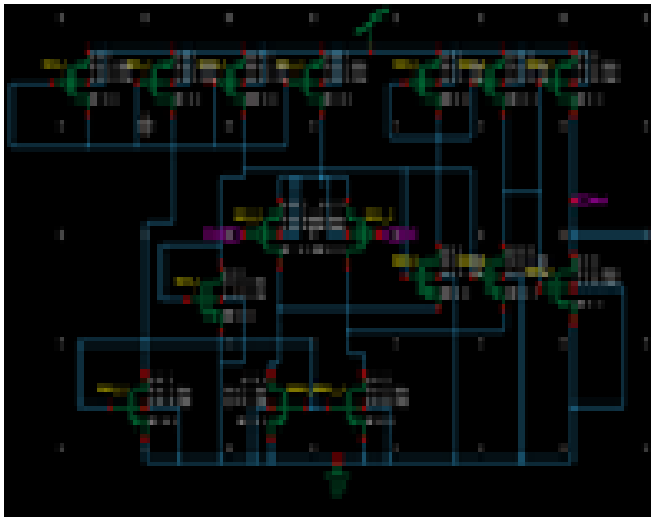
The categories of Opamp measurements and simulation include open loop frequency response (include gain, phase margin), input offset voltage, common-mode gain, Power supply rejection ratio, common mode input and output voltage ranges & transient response including slew rate.

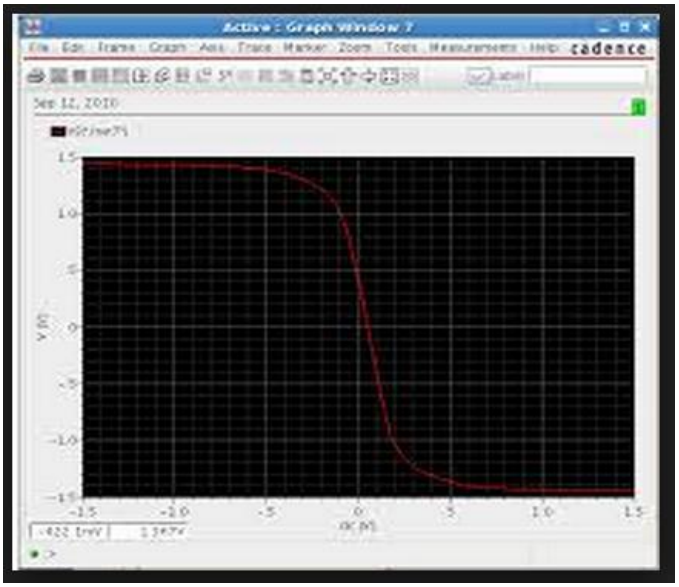
Specification:

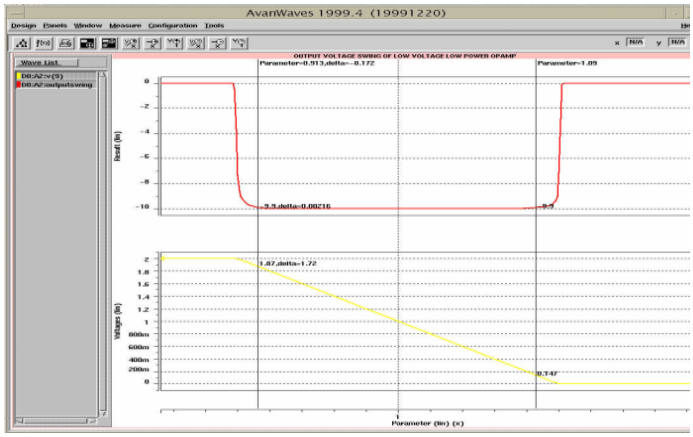
Operating temperature = 27°C Positive Power Supply = 2V Negative Power supply = 0

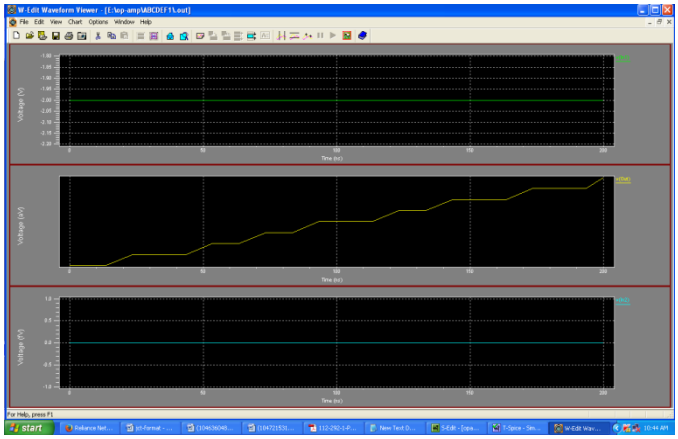
Cload = 10pf

Table-4.3 Specification of LVLP OpAmp

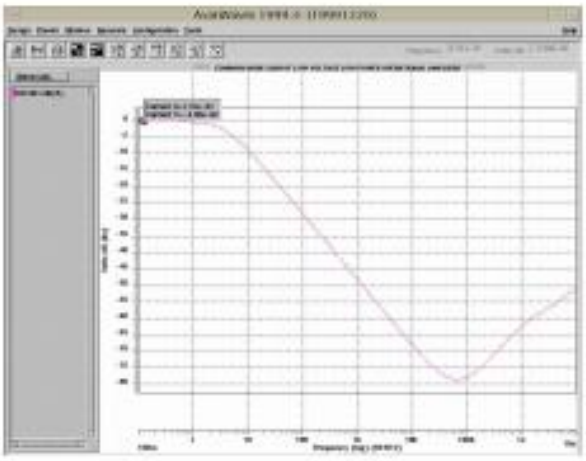








Parameter	Value
UGB	480kHz
Input bias current	1μA
Total supply current	12.877μA
Total power dissipation	25.754mW
DC gain	102dB
Phase margin	60.35°
Input common mode range	-0.35V to 1.13V
Input offset Voltage	0.00025mV
Output Swing	0.147V to 1.87V
CMRR	102.00438db
Common Mode Gain	-0.00438db
Slew rate(Rise)	0.2V/μs
Slew rate(Fall)	0.21V/μs
PSRR(+)	59.7db
PSRR(-)	59.7db
SettlingTime (Rise/Fall) (1%)	4.7μs /4.6μs



Common Mode Gain

Comparison

Comparison of performance of various op amp topologies

	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

4.CONCLUSION AND FUTUREWORK:

As the analog content of large mixed signal integrated circuits increases, it is important to reduce power dissipation. Opamp for minimum power dissipation is required for the required performance along with the means of increasing the output current when driving large capacitive loads. It was seen that a low power opamp could be obtained at the expense of frequency response and other desirable characteristics. Most low power opamp work in weak inversion mode to reduce power dissipation and therefore perform like BJT opamp circuits.

As the power-supply voltages because of the technology improvement and it are desired to reduce power supply to minimize power dissipation, many challenges face the analog designer. One is to keep noise level as possible. The opamp must be designed to with the ever decreasing power supply voltages. As the power supply voltages begin to approach 2Vt , new technique and new opamp topology like folded cascode should be used.

Folded cascode opamp is a better solution for low voltage low power operation as compared to conventional opamp. It provide large ICMR and better frequency performance which is required for low voltage operation and can be designed for low power operation also.

ACKNOWLEDGMENT

I am very thankfully to KIET College for providing a good lab facility. We simulate the Result on ***TANNER TOOLS V 13.0***

REFERENCES

[1] Phillip E. Allen, Benjamin J. Blolock and Grabiel A. Rincon “Low Voltage Analog circuit using standard CMOS technology”

[2] Johan H. Huijsing, Senior Member, Ron Hogervarst and Klass-Jan de Langen “Low Power Low Voltage VLSI OPAMP cells” IEEE Transaction on circuits and sytems, vol-42, No-11, p.p 841-852, Nov 95.

[3] Eric Vittoz and Jean Fellrath “CMOS Analog Integrated Circuits Based on Weak Inversion Operation” IEEE JSSC, vol, SC-12, No-3, p.p. 224- 231, June 1997.

[4] R. R Troutman and S. N. Chakravarti“Subthreshold characteristics of Insulated gate field effect transistor” IEEE transactions Circuit Theory, vol CT-20, pp 659-665,Nov 1973

[5] M.Degrauwe, E.Vittoz & I.Verbauwhede“A Micropower CMOS- Instrumentation Amplifier” IEEE JSSC, vol, Sc-12, pp 805-807, June 1985

[6] Haluk Kulah and Tayfun Akin “A Current Mirroring Integration Based Readout circuits for high performance infrared circuits for high Performance infrared FPA application”.IEEE transactions on circuits And systems-II Analog and digital signal processing, vol-50.

[7] Antonio J lopez-Martin, Sushmita Baswa, Jaime Ramirez-Angula and Ramon Gonzalez Carvajal“Low Voltage Super Class AB CMOS OTA Cells with very high slew rate and Power efficiency”.IEEE JSSC, vol-40, No-5, pp-1068-1077, May2005.

[8] R.Harjani, R.Heinekeand F.Wang. “An Integrated Low-Voltage Class AB CMOS OTA” IEEE JSSC, vol-34, no-2, p.p. 134-142, Feb-1999.

[9] S.Baswa, A.J Lopez-martin, J.Ramirez-Angula, and R.G.Carvajal "Low Voltage Micropower Super Class AB CMOS OTA" Electronic Lett. Vol-34, no-2, p.p134-142, Feb-1999.
[10] G.Palmisano and Pennisi "A true Low-Voltage CMOS Class AB Current Mirror" ISCAS-2000 IEEE International Symposium on Circuits and systems, May 28-31, 2000
[11]http://edaboard.com
[12] Kang, Sung-Mo, Leblebici and Yusuf (1999),"CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill International Editions, Boston, 2nd Edition.
[13] A. P. Chandrakasan el al., "Low-power CMOS digital design," IEEE Journal of Solid-state Circuits", Vol. 27, pp. 473-484, Apr. 1992.

Authors Profile:

Lakshmi Sunanda. Chikkala *is a final year student of M.Tech VLSI System Design in Kakinada Institute of Engineering and Technology, Korangi, Andhra Pradesh, India. He obtained his Bachelor Degree in Engineering (Electronics and Communication) from Regency Institute of Technology, Yanam, India, in 2011. His area of research includes designing of low power memories at micrometer regime, low power VLSI design, analog & digital integrated circuit design, embedded system.*

Gannanaga Prasad Nandipati *completed his B.Tech in Electronics and Instrumetation Engineering in 2005 and M.Tech in VLSI System Design in 2011 from Kakinada Institute of Engineering and Technology, Korangi, Andhra Pradesh, India. He was responsible for teaching and research in VLSI to post graduate students. Currently he is working as a Assistant Professor in Kakinada Institute of Engineering and Technology from two years. His research areas include low-voltage, low power, and high-performance integrated circuit design and simulation of Very large scale integrated circuits.*

D.Mahesh varma *completed hisM.Sc in Electronics from DNR college of Education, Bhimavaram, India in 2005.And M.Tech in VLSI Design from Sathyabama University, Chennai, India in 2008. Currently he is working as a Assistant Professor in Kakinada Institute of Engineering and Technology from four years. His research areas include low power VLSI, LAYOUT design, leakage reduction, sensor networks, energy-efficient circuits, memory design, and sub-threshold operation.*

