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Design of Chip for Flash ADC application of MCML in 180nm Technology

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ABSTRACT--This report describes how MOS Current-Mode Logic (MCML) based circuits components where designed and created, in order to implement a six bit flash ADC. A short introduction about MCML circuits is given, as well as a complete description of speed-to-power ratio of MCML is compared to CMOS counterparts. Design was done in a 0.18 um CMOS technology.

In a modern communication receiver, the received signal is quantized by an analog-to digital converter (ADC) so that complex signal processing can be performed in the digital domain.

keywords-Tainer Eda software, code for programing , layout of the designing

I. Introduction

With the merits of digital circuits that provide a strong incentive to make the world digital, two aspects of our physical environment impede globalization. Firstly the naturally occurring signals are analog and secondly human beings perceive and retain information in analog form. When digital signals are corrupted by the medium such that they become comparable with noise, it is often necessary to treat them as analog signals .

Broadband communications are ubiquitous for providing high-data rate services such as high-speed internet access and future interactive TV. High-bandwidth communications are demanded to accommodate rapid growth of the worldwide network. There are two types of the communication media: wireline and wireless. Typical communication systems of those two medias for wideband data rate are Very High-Speed Digital Subscriber Lines (VDSL) and digital radio **.[1]**

II. SCHEME OF MCML

When designing High-Speed ICs with classical CMOS technology we encounter the problem that delay limits the switching speed of the gate. We can improve the propagation delay times via correctly sizing our transistor, as large W/L ratios will result in a faster switching gate, but also in bigger power consumption. Some techniques developed to improve

the design of High-Speed circuits (as Complementary Pass-Transistor Logic (CPL) or Differential Cascode Voltage Switch Logic (DCVSL)) showed that when differential signals are used in the circuits, a compact design, a better noise immunity and, in short, a better gate for this kind of High-Speed operation can be obtained.

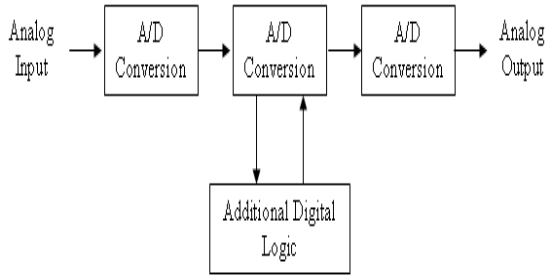
MOS Current-Mode Logic circuits provide true differential operation, have the feature of low noise level generation, and have static power dissipation: the amount of current drawn from the power supply does not depend on the switching activity. Due to this, MCML gates have been discovered to be useful for analog and mixed-signal ICs**.[2]**

III. Data Conversion's Principles

Data conversion is an essential aspect of any signal processing system. It can be divided into two parts: analog-to-digital (A/D) and digital-to-analog (D/A) conversion.

An analog input signal is sensed from the "outside world" (i.e., voice) and processed by the analog-to-digital converter (ADC). The ADC takes the analog signal and gives a digital representation which is defined over a finite set of values in amplitude and time. Once the input is in digital form, the data can be

processed by the digital-signal processor (DSP). Depending on the application, additional digital logic might be interfaced to the DSP to provide extra processing functions to the system. After the data is processed, it is converted back into analog form by the digital-to-analog converter (DAC). **[3]**



Block Diagram of a Signal Processing System.[3]

IV. Analog to Digital converters Sub ranging

A sub ranging ADC uses fewer comparators than parallel flash ADCs. Instead of using one comparator per LSB like a flash converter does, a sub ranging ADC uses fewer comparators, draws less power, has lower input capacitance, and can attain higher resolutions. Although not as fast as a parallel ADC, sub ranging (also called pipelined) ADCs can digitize at speeds greater than 100Msamples/s at 8-bit resolution. They can resolve signals to 16 bits at slower speeds. Sub ranging ADCs often find use in RF test equipment, lower-speed digitizing oscilloscopes, and high-end PC plug-in digitizer cards and PC-external data-acquisition systems.
Figure 2.9 shows a block diagram of an 8-bit sub ranging ADC that uses two 4-bit stages to digitize the analog input signal. The first ADC converts the upper 4 bits while the second stage converts the lower 4 bits. This design uses 30 comparators (15 for each ADC) rather than the 255 comparators required by an 8-bit flash converter. A 12-bit sub ranging ADC may use two 6-bit stages, three 4-bit stages, or four 3-bit stages**.[3]**

V. ADC Circuit Blocks

In Chapter 2 the basic concepts of data conversion were presented and a number of architectures commonly employed for A/D conversion were described. The S/H circuit, the D/A converter, and the comparator were presented as fundamental components for the operation of an ADC.

The main performance metrics of each circuit block are described along with different techniques available for the implementation of these circuits.

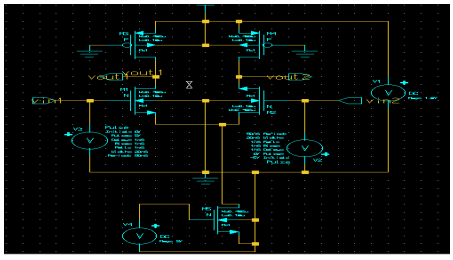
A sample-and-hold (S/H) circuit takes samples of its analog input signal and holds these samples in a memory element. The key feature of this circuit, when used as the front end of an ADC, is that it relaxes the timing requirements of the latter. This means that the precision and speed of the converter will be limited to a certain degree by the S/H circuit.

The operation of a S/H circuit is divided into two modes, sample and hold. Usually this is done at uniform time intervals, set by a periodic clock that divides circuit operation into two phases. During the sample-mode the output of the circuit can either track the input or reset to some fixed value. In the hold-mode, the output of the S/H circuit is equal to the input value obtained (sampled) at the end of the sample mode. Figures 3.1 (a) and (b) illustrate example waveforms for a S/H circuit and a T/H (track-and-hold) circuit. Although here a distinction was made between sampling and tracking, the majority of the circuits are referred to as S/H circuits even though they behave as T/H circuits.
The most basic form of a S/H circuit combines a switch and a capacitor, as shown in Figure 3.2. The operation of the circuit proceeds as follows. In sampling mode the switch is “on”, creating a signal path that allows the capacitor to track the input voltage. When the switch is “off” an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into holding mode**.[4]**

VI. MOS Current-Mode Inverter

This inverter uses four MOS transistors, two PMOS and two NMOS , This circuit does a current to voltage conversion. **[6]**

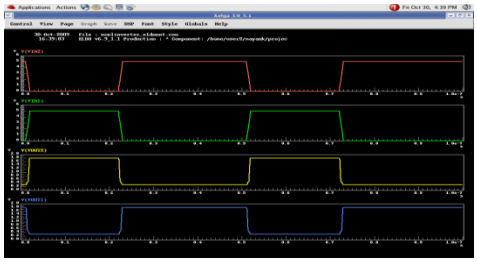
Schematic of MCML Inverter



- **Input Parameter**
  - L_N = 0.18um

- W_N = 0.54um
- L_P = 0.18um
- W_P =1.08um
- Pulse = 0 to1.2V
- Rise time = 1ns
- Fall time =1ns
- Width = 20ns
- Period = 40ns

Waveform of MCML inverter



Our procedure

(A) Steps

1. USE S/H circuits, D/A converters, and comparators and collect required data.

2 .. After collecting required data use **Tainer EDA** software for implementation of MCML design.

3. First of all **S-spice** use for schematic diagram of designing.

4. Then **T-spice** use for the transent simulation for giving input and output variables.

5. Then for finding output waweform use **W-spice** for simulation**.**

6.Then performance specifications, as obtained from Spice simulations, are presented.

7. Resolution, Speed & Power by the designing MCML obtained for analog to digital convertor's.

(B) Discussion

1. Designing of MCML

In contrast, MCML produces a small switching noise because the current supplied by V_{DD} during switching is almost constant. Moreover, owing to their differential structure, MCML gates exhibit a better noise immunity with respect to complementary CMOS logic**.**

MOS Current Mode Logic (MCML) has been proved to be preferable to complementary CMOS in mixed signal environment. The main reason for that is the large amount of switching noise introduced by complementary CMOS. This adversely affects the accuracy of the analog section in mixed signal IC's. The present paper investigates the dependence of I_B and ΔV on the constraints on area and delay. More specifically, we will show that the constraint on the area may affects the lower limit of ΔV and the upper limit of I_B whereas the constraint on the delay sets a lower limit on I_B**.**

Moreover, methods will be presented for computing such limits. The method for finding the minimum bias current is based on the concept of crossing point current.

2. MCML IINVERTER'S SPEED

When designing High-Speed ICs with classical CMOS technology, we encounter the problem regarding delay limits for the switching speed of the gate. We can improve the propagation delay times via correctly sizing our transistor, as large W/L ratios will result in a faster switching gate, but also large power consumption, as we observed in our experiment. Some techniques developed to improve the design of High-Speed circuits (as Complementary Pass-Transistor Logic (CPL) or Differential Cascade Voltage Switch Logic (DCVSL)) showed that when differential signals are used in the circuits, a compact design, a better noise immunity and, in short, a better gate for this kind of High-Speed operation can be obtained.

MOS Current-Mode Logic circuits provide true differential operation, have the feature of low noise level generation, and have static power dissipation**:**

Resolution, Speed & Power Requirements for Popular ADCs.

	Low Resolution (6-10 bits)	**Medium Resolution (10-16 bits)**	**High Resolution (16-20 bits)**
ΔΣ -speed -power	-n/a -n/a	128S/s-40kS/s 0.27 - 122mW	12S/s-105kS/s 0.6 -35mW
SAR -speed -power	20kS/s - 1MS/s 0.6 -250mW	40kS/s - 1.25MS/s 1.95 - 200mW	n/a n/a
Pipeline -speed -power	2MS/s - 105MS/s 0.6 -250mW	40kS/s - 1.25MS/s 250 - 1200mW	n/a n/a

It can be seen that the best trade-off between speed and power consumption is achieved by the SAR ADC. It achieves higher conversion speed than the .S ADC while consuming less power than the Pipeline ADC.

IX. Result and Conclusion

The various model of MCML based component which will used in MCML Flash 6 bit ADC. The switching time verses power dissipation comparison of MCML and CMOS circuit component is at 0.18-um technology.

This study shows the various aspects of designing ultra high speed circuits with MCML which has better power-speed tradeoffs than CMOS circuit's at GHz-range frequency. Moreover, its resolution range is similar to that offered by the Pipeline ADC. It achieves higher conversion speed than S ADC, while consuming less power than the Pipeline ADC which is better for MCML rather than CMOS is shown in below table

Table 6: Comparison of 0.18-um MCML and CMOS circuit component:

Circuit Component	**Design Method**					
	MCML			**CMOS**		
	DC Supply	**Switching Time(ns)**	**Power Dissipation**	**DC Supply(V)**	**Switching Time**	**Power Dissipation**
Inverter	1.2	0.3	274.649	1.2	22	23.72
OR-NOR	1.2	9	915.63	1.2	24.5	26.54
X-OR	1.2	0.7	365.63	1.2	1.6	34.088

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