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An Improve I2C Protocol For Secure Multiuser Data Transmission

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***Abstract*—When using the I 2C bus protocol, the designer must ensure that the hardware complies with the I 2C standard. This application report describes the I2C protocol and provides guidelines on debugging a missing acknowledgment, selecting the pullup resistors, or meeting the maximum capacitance load of an I2C bus. A conflict occurs if devices sharing the I2C bus have the same slave address. This document provides solutions to this conflict by using the devices' features or external components Inter-integrated circuit (I2C) (NPX) is a two-wired protocol that can operate at different speeds (standard mode, fast mode, and high-speed mode). Although other protocols are simpler and do not have speed limitation (such as SPI), the scalability offered by I2C made it attractive as an interface for some of TI's CDC products. I2C prevents data corruption by performing a wired-AND operation as the I2C interface has open-drain or open-collector output. When the SDA line is low that translates in the I2C bus as being busy. Also, this interface allows the master to check the bus status. By pulling the master SDA line high, it can verify the status of the bus: busy if the line stays low (as some device is pulling the line low), or free if the line is high.**

***Keywords*- I 2C bus protocol, SDA line, SPI and NPX etc**

I. INTRODUCTION

Information with significant meaning when exchanged among two entities is termed as communication. Communication can happen between two or more than two humans, or between two or more than two living things, or between two or more than two devices. Communicators, Medium, Language and speed are the basic requirement for a communication to take place. For example when two persons are communicating, then for a significant communication both of them must be able to speak and listen, secondly there must be a medium (air) to let their voice propagate through space to each other's ears, thirdly their conversation must take place in a language understood by both of them and last but not the least the speed at which they are communicating must be synchronized so that conversation is understood able by both of them.

The above mentioned requirements are a must not only in the case of human being but also among all sort of communication. Thus when a communication takes place between two electronic devices the same holds the governing within the process.

1.1 Types of Communication System

The communication system can be classified according to their physical infrastructure and specifications of signals they transmit. The physical infrastructure concerns the used channel type and the hardware design of the transmission and receiving equipment. The signal specifications mean the nature and type of the transmitted signal. The types of communication systems on the basis of their infrastructure and signal specifications are described below.

1.2 Serial Peripheral Interface Bus

The Serial Peripheral Interface (SPI) bus is a specification of synchronous serial communication interface utilized for short distance communication, primarily in embedded systems. The interface was established by Motorola and turn out to be a de- facto standard. Typical applications consist of Secure Digital and LCD screens.

SPI devices communicate in full duplex mode using a master-slave architecture with one master. The master device is from the framework for reading and writing. Multiple slave devices are maintained by the selection with selected individual slaves (SS) lines.

Sometimes SPI serial bus is called a four son, contrasting with three, two and one wire serial bus. The SPI can be defined as a synchronous serial interface, but it is differ from the serial interface (SSI) synchronous protocol, which is a synchronous serial communication protocol to four son, but employs differential signalling and provides a single channel simplex communication.

1.3 I2C bus (Inter IC bus)

The I2C (Inter IC) is a serial bus with two bidirectional son that provides a communication link between integrated circuits (ICs). Phillips introduced the I2C bus 20 years ago for mass-produced items such as TVs, VCRs and audio equipment. Today, I2C is the de-facto solution for embedded applications. There are three data transfer speeds for the I2C bus: standard, fast mode and the high speed mode. Standard is 100 Kbps. Fast mode is 400 Kbps, and the high speed mode supports speeds up to 3.4 Mbps. All are backward. The I2C bus supports devices and devices that operate under different spatial tensions and 7bit 10bit address.

II. LITERATURE SURVEY

Wamkeue, K. Gavaskar, et. al, [2017], The I2C Master Controller bus was successfully designed using Verilog and Simulated. The Verification Environment was created using System Verilog. The proposed verification environment comprised of interface, generator, monitor, driver and scoreboard were implemented by using OOP concepts. The functionality of the design is verified by the System Verilog Verification Environment. The constrained randomization technique is applied for the design and verification environment. The functional coverage obtained was 100% by using the cover groups. The code coverage obtained for DUT was 92.38% and the code coverage obtained for the Top Module in Verification process was 92.90%. This can be further extended for multiple masters. Further, it can be used to check whether the data sent by the master is received by slave. [01]

K.B. Bharath, et. al. [2016] – This shows the working of an I2C protocol for multiple master-multiple slave configuration operation. Arbitration technique has been implemented by satisfying DO-254 standards. When multiple masters are taken into consideration in an I2C structure design it is necessary to know which master holds the bus and for this the authors had utilized arbitration technique along with DO-254 standards so as to satisfy the reliability, reusability and assurance for the design. In order to implement the same Reqtracer, HDL Designer, QuestaSim, and precision RTL Plus tools are used at different phases of the FPGA flow. Arbitration refers to the cancelling the communication of one master if other master is communicating with the slave. As per the progress shown in the work done by the author in this area it's been identified that the arbitration can take place during the start condition of the I2C and during the data transmission. In an I2C physical wiring structure both the clock and data line are connected to Vdd through pull up resistor, which ever master pulls the data line low, that master gets the arbitration. This is excluded by some of the cases where both the masters pull the data line low simultaneously and there may be loss of communication when both the master keeps on sending the data as they had got the bus. After some time when the master tries to pull the data low but data line is already sensed as low then the master's loos the bus and cancel the communication.

AnaghaA, M. Mathurakaniet. al, [2016] –In this project work, the multi-master facility of I2C Protocol is implemented successfully. Address resolution is the major concern while using multiple masters in I2C bus. Arbitration procedure must be perfect for the bus to work properly when dual masters are present. A dual master I2C bus controller system with an EEPROM 24CXX series as the slave devices has been developed for realizing both the read and write cycles of the I2C bus and tested. The design has got successfully implemented in Spartan 3A FPGA and the outputs are verified. Also DS1307 RTC is connected as the slave device and performed the WRITE and READ operations following I2C protocol. This design can be used in systems where multiple devices needs to be interconnected by ensuring with low complexity and efficient resource utilization.[03]

Bollam, Eswariet. al. [2013]. This implements the serial data communication using I2C (Inter-Integrated Circuit) bus master controller using a field programmable gate array (FPGA). The I2C bus master controller is interfaced with MAXIM DS1307, which act as a slave. This module was designed in Verilog HDL and simulated in Model SIM 10.1c. The design was synthesized using Xilinx ISE Design Suite 14.2. I2C master initiates the transmission of data and the slave responds. It can be used to interface devices at low speed as motherboard, embedded system, mobile phones, set-top boxes, DVD, other electronic devices or PDAs. In their work, they designed an I2C master controller using HDL Verlilog based on Finite State Machine (FSM). [04]

III. PROPOSED ALGORITHM

This research is based on the hardware description done on Xilinx ISE with VHDL mixed modeling style along with an efficient Finite State Machine used to implement the required flow for multi device interface.

4.1 Design Entity

I2C communication protocol at the master device side needed to be implemented using the VHDL. The timing diagram described in the I2C master end we needs change in the physical voltage stage of the SDA signal in reference to the

SCLK signal. As for the new approach we are interfacing more than one slave device simultaneously through the same FPGA master device, the entity of the new master device will be modified along with the needed data to be send over the I2C line. Below figure shows the proposed entity of the design.

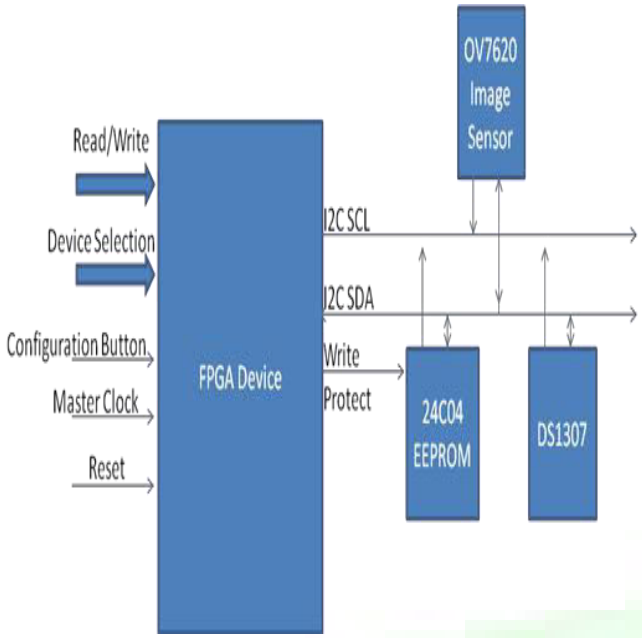

Figure 1: Proposed entity of the design

The master device used over here is XILINX FPGA from SPARTAN6 family. Input given to the FPGA master either using tact switches or sliding switches. Main inputs are the Read/Write button to decide whether the master will write to the communicating device or read from the communicating device. It's a single bit input with following circuit.

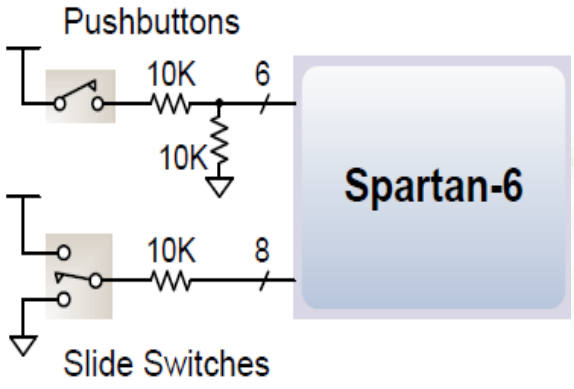

Figure 2: single bit input

Similarly slide switches are used to select the targeted slave device among the there. Configuration switch needed to send the register values to write them on the slave devices if needed. And the last reset button to reset the complete device to start from the scratch of the encoded function.
Main clock given to the FPGA device is given from an oscillator source as shown in the below schematic.

The SPARTAN 6 board includes a single 100 MHz CMOS oscillator connected to pin L15. This is used as the main clock source for the complete setup. Frame format of the I2C protocol gives the basis for creation of the flow diagram i.e. the state machine for each sort of frames to be implemented in the design.

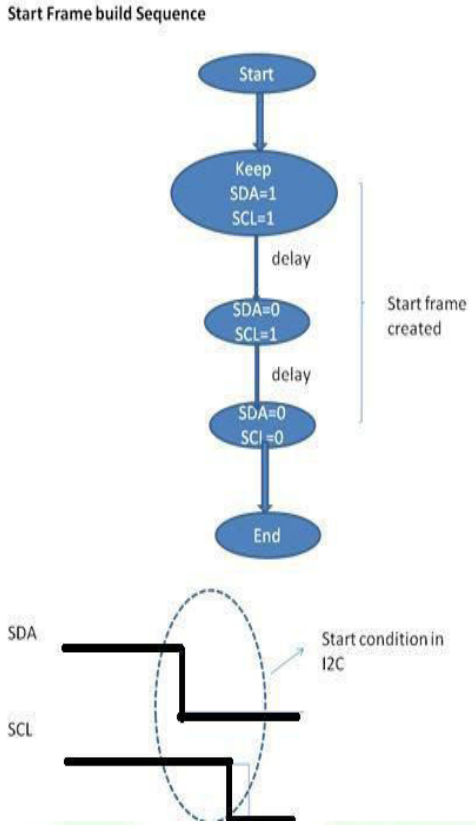

Figure 3: Start Frame for I2C protocol

Similarly the stop frame for the protocol is designed as per I2C specification by changing the logical values of SDA and SCL.

V. Simulation and Result

The output and the result of the proposed method is show in the Model Sim. Model Sim is a multi-language HDL simulation environment by Mentor Graphics, for the simulation of hardware description languages such as VHDL, Verilog and System C, C and includes a built-in debugger. Model Sim can be used independent or jointly with Altera Quartos or Xilinx ISE. Performed simulation uses the graphical user interface (GUI) or automatically using scripts. Commented design steps in the last chapter were followed to implement the design of Multi implementation of the I2C device interface for Bus Master Controller on FPGA. Below are the various tables generated After-Master I2C Bus Controller synthesize design.

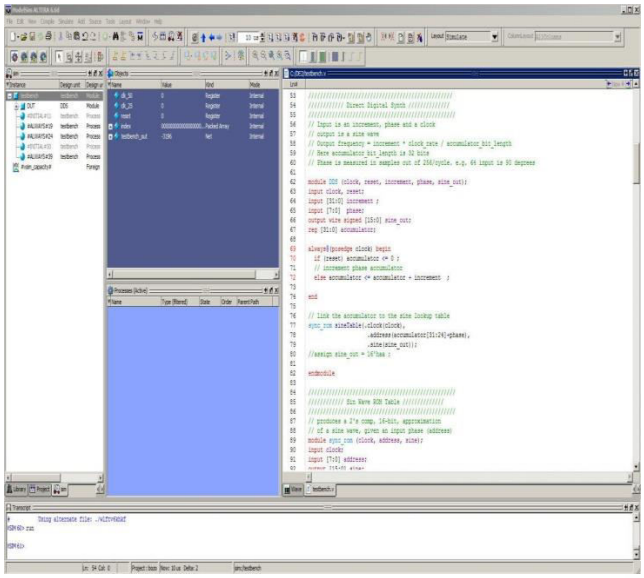

Fig. 4 **Device Selection for communicating with the I2C Master Bus Controller**

For the multi device communication of the I2C master controller firstly the device had to be selected and for the purpose to show the working of design we had simulated the synthesized design using the integrated simulation software in XILINX. Further implemented the different read and write operations on various devices by selecting their respective read-write addresses. Figure 5.2 shows the VHDL coded Model Sim output of device selection.

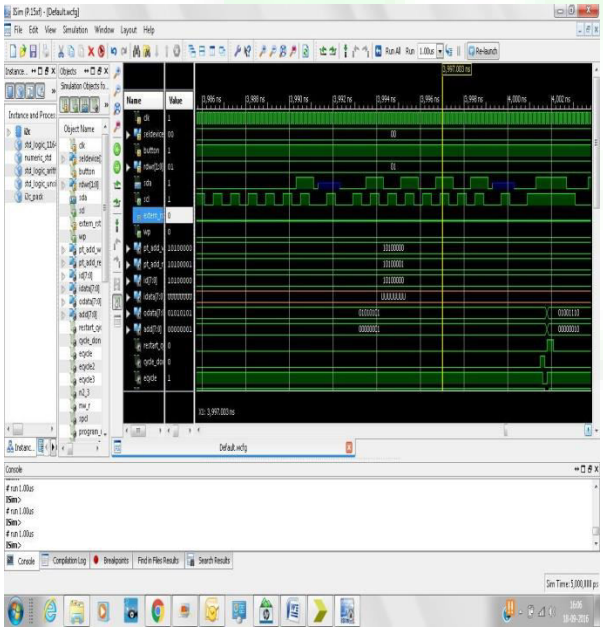

Figure 5: Shows the Device Selection (EEPROM) with write operation

All Xilinx Block is a powerful modeling tool that allows digital complex systems to be designed using a block diagram methodology. The System Generator enables the modeling of digital systems, which can be transformed into Model Sim atmosphere and focused on a Xilinx FPGA board. Bit stream automatic generation is supported with synthesis tools and implementation in the run Model Sim and the Xilinx environment. The design is checked and tested in both ISE / Model Sim Xilinx and Impact. The system is studied by real-time hardware implementation with Spartan 6 FPGA, image sensor OV7620, 24C04 EEPROM IC and DS1307 RTC device. Integrated circuits at high speed Hardware Description Language (VHDL) can be used to model a digital system at several levels of abstraction ranging from the algorithmic level to the gate level with a high degree of complexity. The simulation

Integrated circuits at high speed Hardware Description Language (VHDL) can be used to model a digital system at several levels of abstraction ranging from the algorithmic level to the gate level with a high degree of complexity.

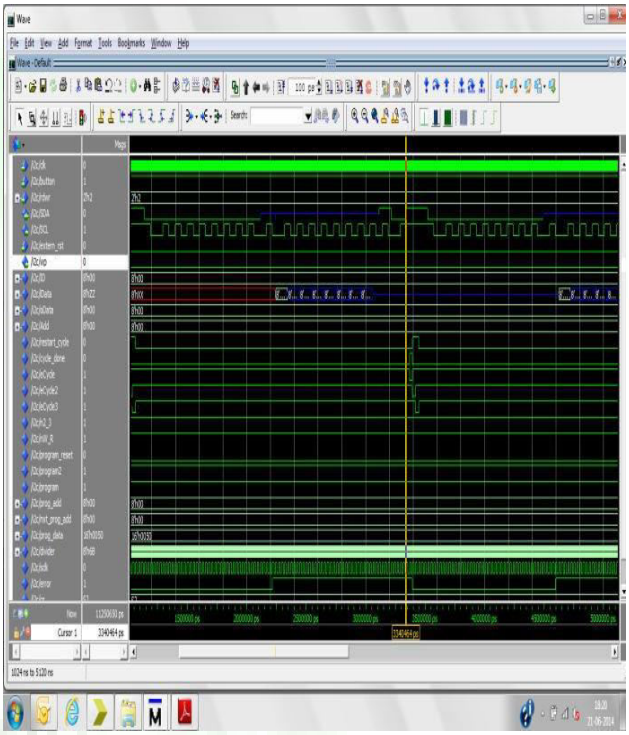

Figure 6: Final output of proposed System on Model Sim

VI. Conclusion

This research work shows an efficient implementation of Multi Device I2C interface using FPGA as Master Device. Research work describes the utility of FSM implementation in HDL coding and also shows the improvement in the architecture formed for the protocol implementation in reconfigurable devices.

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