Hybrid Converter Topology with AC Drive Using Fuzzy logic Technique

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Abstract— **This paper proposes a single-phase to three-phase drive system composed of two parallel single-phase rectifiers, a three-phase inverter, and an induction motor. The proposed topology permits to reduce the rectifier switch currents, the harmonic distortion at the input converter side, and presents improvements on the fault tolerance characteristics. The complete comparison between the proposed fuzzy control strategy and PI control strategy of hybrid converter topology has been carried out in this paper. Compared to the conventional topology, the proposed system will reduce the rectifier switch currents, the *THD* of the grid current with same switching frequency. The results are discussed clearly.**

Index Terms—**Ac-dc-ac power converter, drive system, parallel converter's, Fuzzy Controller**

1. INTRODUCTION

Several solutions have been proposed when the objec-tive is to supply three-phase motors from single-phase ac mains [1]–[9]. It is quite common to have only a single-phase power grid in residential, commercial, manufacturing, and mainly in rural areas, while the adjustable speed drives may request a three-phase power grid.

Single-phase to three-phase ac–dc–ac conversion usually employs a full-bridge topology, which implies in ten power switches, as shown in Fig. 1. This converter is denoted here as conventional topology.

Parallel converters have been used to improve the power capability, reliability, efficiency, and redundancy. Parallel converter techniques can be employed to improve the performance of active power filters [10]–[13], uninterruptible power supplies (UPS) [14]–[16], fault tolerance of doubly fed induction generators [17], and three-phase drives [18], [19]. Usually the opera-tion of converters in parallel requires a transformer for isolation. However, weight, size, and cost associated with the transformer may make such a solution undesirable [20]. When an isolation transformer is not used, the reduction of circulating currents among different converter stages is an important objective in the system design [21]–[26].

In this paper, a single-phase to three-phase drive system com-posed of two parallel single-phase rectifiers and a three-phase

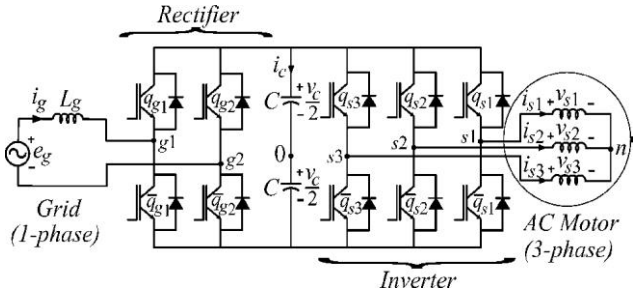

Fig. 1. Conventional single-phase to three-phase drive system

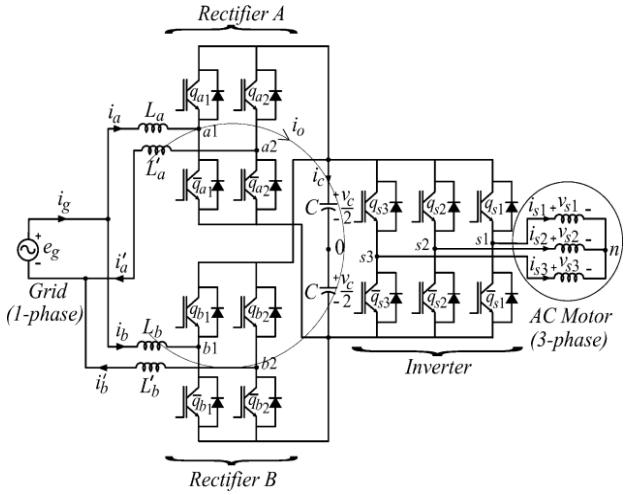

Fig. 2. Proposed single-phase to three-phase drive system

Inverter is proposed, as shown in Fig. 2. The proposed system is conceived to operate where the single-phase utility grid is the unique option available. Compared to the conventional topology, the proposed system permits: to reduce the rectifier switch currents; the total harmonic distortion (*THD*) of the grid current with same switching frequency or the switching frequency with same *THD* of the grid current; and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart. The aforementioned benefits justify the initial

investment of the proposed system, due to the increase of number of switches.

II. SYSTEM MODEL

The system is composed of grid, input inductors **(** L_a **,** L_a^I **,** L_b **and** L_b^I**),** rectifiers (A and B), capacitor bank at the dclink, inverter, and induction machine. Rectifiers A and B are constituted of switches $q_{a1}, \overline{q}_{a1}, q_{a2}$ and $\overline{q}_{a2}$ and q_{b1} q_{b2} $\overline{q}_{b1}$ $\overline{q}_{b2}$, respectively. The inverter is constituted of switches $q_{s1}, \overline{q}_{s1}, q_{s2}, \overline{q}_{s2}, q_{s3}$ and $\overline{q}_{s3}$. The conduction state of the switches is represented by variable s_{qa1} to s_{qa3}, where s_q =1 indicates a closed switch while s_q =0s an open one.

From Fig. 2, the following equations can be derived for the Front-end rectifier

$$v_{a10} - v_{a20} = e_g - (r_a + l_a \mathrm{p}) i_a - (r_a^1 + l_a^1 \mathrm{p}) i_a^1 \quad (1)$$

$$v_{b10} - v_{b20} = e_g - (r_b + l_b \mathrm{p}) i_b - (r_b^1 + l_b^1 \mathrm{p}) i_b^1 \quad (2)$$

$$v_{a10} - v_{b10} = (r_b + l_b \mathrm{p}) i_b - (r_a + l_a \mathrm{p}) i_a \quad (3)$$

$$v_{a20} - v_{b20} = (r_a^1 + l_a^1 \mathrm{p}) i_a^1 - (r_b^1 + l_b^1 \mathrm{p}) i_b^1 \quad (4)$$

$$i_g = i_a + i_b = i_a^1 + i_b^1 \quad (5)$$

Where p = $\frac{d}{dt}$ and symbols like r and l represent the

Resistance and inductances of the input inductors L_a , L_a^1 , L_b , and L_b^1 .

The circulating current i_o can be defined from i_a and i_a^1 or i_b and i_b^1 ,i.e.,

$$i_o = i_a - i_a^1 = - i_b + i_b^1 \quad (6)$$

Introducing i_o and adding (3) and (4), relations (1)—(4) become

$$v_a = e_g - [r_a + r_a^1 + (l_a + l_a^1) \mathrm{p}] i_a + (r_a^1 + l_a^1 \mathrm{p}) i_o \quad (7)$$

$$v_b = e_g - [r_b + r_b^1 + (l_b + l_b^1) \mathrm{p}] i_b + (r_b^1 + l_b^1 \mathrm{p}) i_o \quad (8)$$

$$v_o = - [r_a^1 + r_b^1 + (l_a^1 + l_b^1) \mathrm{p}] i_o - [r_a - r_a^1 + (l_a - l_a^1) \mathrm{p}] i_a + [r_b - r_b^1 + (l_b - l_b^1) \mathrm{p}] i_b \quad (9)$$

Where

$$v_a = v_{a10} - v_{a20} \quad (10)$$

$$v_b = v_{b10} - v_{b20} \quad (11)$$

$$v_o = v_{a10} + v_{a20} - v_{b10} - v_{b20} \quad (12)$$

Relations (7)–(9) and (5) constitute the front-end rectifier Dynamic model. Therefore, v_a (rectifier A), v_b (rectifier B), and v_o (rectifiers A and B) are used to regulate currents i_a , i_b and i_o , Reference currents i_a^* and i_b^* are chosen to i_g^* /2 and t he reference circulating current i_0^* is chosen equal to 0

In order to both facilitate the control and share equally current, Voltage, and power between the rectifiers, the four inductors should be equal, i.e., $r_g^1 = r_a = r_a^1 = r_b = r_b^1$ **and** $l_g^1 = l_a = l_a^1 = l_b = l_b^1$. In this case, the model (7)–(9) can be simplified to the model given by

$$v_a + \frac{v_0}{2} = e_g - 2(r_g^1 + l_g^1 \mathrm{p})\ i_a \quad (13)$$

$$v_b - \frac{v_0}{2} = e_g - 2(r_g^1 + l_g^1 \mathrm{p})\ i_b \quad (14)$$

$$v_o = -2(r_g^1 + l_g^1 \mathrm{p})\ i_o \quad (15)$$

Additionally, the equations for i_g , i_a^1 and i_b^1 can be written as

$$v_0 = v_{a10} + v_{a20} - v_{b10} - v_{b20} \quad (19)$$

When i_0 =0 ($i_a = i_a^1, i_b = i_b^1$) the system model (7)–(9) is Reduced to

$$v_a = e_g - 2(r_g^1 + l_g^1 \mathrm{p})\ i_a \quad (20)$$

$$v_b = e_g - 2(r_g^1 + l_g^1 \mathrm{p})\ i_b \quad (21)$$

Then, the model of the proposed system becomes similar to that of a system composed of two conventional independent rectifiers.

III. PWM STRATEGY

The inverter can be commanded by using an adequate pulse width modulation (PWM) strategy for three-phase voltage source inverter (VSI) [19], so that it will not be discussed here. In this section, the PWM strategies for the rectifier will be presented. The rectifier pole voltages $v_{a10}, v_{a20}, v_{b10}$ **and** v_{b20} depend on the conduction states of the power switches, i.e.,

$$v_{j0} = (2 s_{qj} - 1) \frac{v_c}{2} \quad \text{for } j = a1 \text{ to } b2 \quad (22)$$

Where v_c is the total dc-link voltage

Considering that v_a^*, v_b^* and v_o^* denote the reference voltages Determined by the current controllers (see Section IV), we found

$$v_a^* = v_{a10}^* - v_{a20}^* \quad (23)$$

$$v_b^* = v_{b10}^* - v_{b20}^* \quad (24)$$

$$v_o^* = v_{a10}^* + v_{a20}^* - v_{b10}^* - v_{b20}^* \quad (25)$$

The gating signals are directly calculated from the reference pole voltages $v_{a10}^*, v_{a20}^*, v_{b10}^*$ and v_{b20}^*. However, (23)–(25) are not sufficient to determine the four pole voltages uniquely from v_a^*, v_b^* and v_o^*. Introducing an auxiliary variable $v_x^* = v_{a20}^*$, that equation plus the three equations (23)–(25) constitute a four independent equations system with four variables ($v_{a10}^*, v_{a20}^*, v_{b10}^*$ and v_{b20}^*). Solving this system of equations, we obtain

$$v_{a10}^* = v_a^* + v_x^* \quad (26)$$

$$v_{a20}^* = v_x^* \quad (27)$$

$$v_{b10}^* = \frac{v_a^*}{2} + \frac{v_b^*}{2} - \frac{v_0^*}{2} + v_x^* \quad (28)$$

$$v_{b20}^* = \frac{v_a^*}{2} - \frac{v_b^*}{2} - \frac{v_0^*}{2} + v_x^* \quad (29)$$

From these equations, it can be seen that, besides v_a^*, v_b^* and v_o^* , the pole voltages depend on also of v_x^*. The limit values. The limit values v_x^* can be calculated by taking into account the maximum $\frac{v_c^*}{2}$ and minimum $-\frac{v_c^*}{2}$ value of the pole voltages

$$v_{x\max}^* = \frac{v_c^*}{2} - v_{\max}^* \quad (30)$$

$$v_{x\min}^* = -\frac{v_c^*}{2} - v_{\min}^* \quad (31)$$

Where v_x^* is the reference dc-link voltages, $v_{\max}^*$ =max V

$v_{\min}^*$ =minV with V= $\{ v_a^*, 0, \frac{v_a^*}{2} + \frac{v_b^*}{2}, -\frac{v_0^*}{2}, \frac{v_a^*}{2} - \frac{v_b^*}{2}, -\frac{v_0^*}{2} \}$

Introducing a parameter μ ($0 \le \mu \le 1$), the variable v_x^* can be written as

$$v_x^* = \mu v_{x\max}^* + (1-\mu) v_{x\min}^* \quad (32)$$

When μ = 0, μ = 0.5, and μ = 1 the auxiliary variable v_x^* has the following values $v_x^* = v_{x\max}^*, v_x^* = v_{xavg}^* = (v_{x\max}^* + v_{x\min}^*)/2$, and $v_x^* = v_{x\max}^*$, respectively. When $v_x^* = v_{x\min}^*$ or $v_x^* = v_{x\max}^*$ a converter leg operates with zero switching frequency.

Once v_x^* is chosen, pole voltages $v_{a10}^*, v_{a20}^*, v_{b10}^*$ and v_{b20}^* .are defined from (26) to (29). The gating signals are obtained by comparing pole voltages with one (v_{t1}), two (v_{t1} and v_{t2}) or more high-frequency triangular carrier signals [27]–[30]. In the case of double-carrier approach, the phase shift of the two triangular carrier signal (v_{t1} and v_{t2}) is 180 ° [see Fig. 5(c) and (d)].

The parameter μ changes the place of the voltage pulses Related to v_a and v_b, when $v_x^* = v_{x\min}^*$ (μ=0) or $v_x^* = v_{x\max}^*$ (μ=1) are selected, the pulses are placed in the begin or in the end of the half period (Ts) of the triangular carrier signal [see Fig. 5(a) and (c)]. On the other hand, when $v_x^* = v_{xavg}^*$ the pulses are centered in the half period of the carrier signal [see Fig. 5(b) and (d)]. The change of the position of the voltage pulses leads also to the change in the distribution of the zero instantaneous voltages (i.e., $v_{a=0}$ and v_b =0) .With μ = 0 or μ = 1 the zero instantaneous voltages are placed at the beginning or at the end of the switching period, respectively, while with μ = 0.5, they are distributed equally at the beginning and at the end of the half period. This is similar to the distribution of the zero-voltage vector in the three-phase inverter [27], [31]. Consequently, μ influences the harmonic distortion of the voltages generated by the rectifier, as it will be shown in Section V.

IV. CONTROL STRATEGY

Fuzzy Logic Controllers:

The word Fuzzy means vagueness. Fuzziness occurs when the boundary of piece of information is not clear-cut. In 1965 Lotfi A.Zahed propounded the fuzzy set theory. Fuzzy set theory exhibits immense potential for effective solving of the uncertainty in the problem. Fuzzy set theory is an excellent mathematical tool to handle the uncertainty arising due to vagueness. Understanding human speech and recognizing handwritten characters are some common instances where fuzziness manifests. Fuzzy set theory is an extension of classical set theory where elements have varying degrees of membership. Fuzzy logic uses the whole interval between 0 and 1 to describe human reasoning. In FLC the input variables are mapped by sets of membership functions and these are called as "FUZZY SETS".

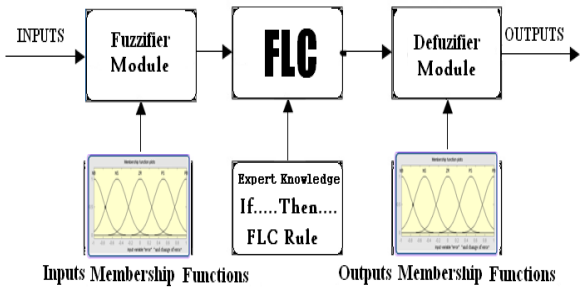

Fig.3.FUZZY BASIC MODULE

Fuzzy set comprises from a membership function which could be defines by parameters. The value between 0 and 1 reveals a degree of membership to the fuzzy set. The process of converting the crisp input to a fuzzy value is called as "fuzzificaton." The output of the Fuzzier module is interfaced with the rules.The basic operation of FLC is constructed from fuzzy control rules utilizing the values of fuzzy sets in general for the error and the change of error and control action. The results are combined to give a crisp output controlling the output variable and this process is called as "DEFUZZIFICATION."

FUZZY RULES:

Control							
e \ Δe	NL	NM	NS	ZR	PS	PM	PL
NL	NL	NL	NL	NL	NL	NL	NL
NM	NL	NL	NM	NM	NS	NS	NS
NS	NL	NM	NM	NS	NS	NS	ZR
ZR	ZR	ZR	ZR	ZR	ZR	ZR	ZR
PS	ZR	PS	PS	PS	PM	PM	PL
PM	PS	PS	PS	PM	PM	PL	PL
PL	PL	PL	PL	PL	PL	PL	PL

Table.2 control strategy based on 49 Fuzzy controls Rule with combination of Seven error states multiplying with seven changes of error states.

Fig. 3 presents the control block diagram of the system in Fuzzy Technique
Fig. 2, highlighting the control of the rectifier. The rectifier Circuit of the proposed system has the same objectives of that in Fig. 1, i.e., to control the dc-link voltage and to guarantee the grid power factor close to one. Additionally, the circulating current i_o in the rectifier of the proposed system needs to be controlled.

In this way, the dc-link voltage v_c is adjusted to its reference value v_c^* using the controller *Rc* , which is a standard PI/Fuzzy type controller. This controller provides the amplitude of the reference grid current I_g^* . To control power factor and harmonics in the grid side, the instantaneous reference current i_g^* must be synchronized with voltage e_g , as given in the voltage-oriented control (VOC) for three-phase system [32]. This is obtained via blocks G_e -- i_g ,based on a PLL scheme. The reference currents i_a^* and i_b^* are obtained by making $i_a^* = i_b^* = \frac{i_g^*}{2}$,which means that each rectifier receives half of the grid current. The control of the rectifier currents is implemented using the controllers indicated by blocks *Ra* and *Rb* . These controllers can be implemented using linear or nonlinear techniques [33]–[37]. In this paper, the current control law is the same as that used in the two sequences synchronous controller described in [38]. These current controllers define the input reference voltages v_a^* and v_b^* The homopolar current is measured (i_0) and compared to its Reference (i_0^* =0) . The error is the input of PI controller R_c that determines the voltage v_0^* . The calculation of voltage is v_x^* given from (30) to (32) as a function of μ, selected as shown in the Section V. The motor there-phase voltages are supplied from the inverter (VSI). Block VSI-Ctr indicates the inverter and its control. The control system is composed of the PWM command and a torque/flux control strategy (e.g., field-oriented control or volts/hertz control).

V. HARMONIC DISTORTION

The harmonic distortion of the converter voltages has been Evaluated by using the weighted *THD* (*WTHD*). It is computed by using

$$WTHD_p = \frac{100}{a_1}$$

Where a_1 the amplitude of the fundamental voltage is, a_i is the amplitude of *i*th harmonic and *p* is the number of harmonics taken into consideration.
Fig. 4 shows the WTHD of voltages generated by rectifiers [$v_{ab} = \frac{v_a + v_b}{2}$ for the proposed configuration and v_g = v_{g10} -- v_{g20} for the conventional one] at rated grid voltage as a function of μ. Note that the parameter μ determine v_x^* From (30) to (32). The resultant voltage v_{ab} generated by rectifier is responsible to control i_g [see (16)], which means that this voltage is used to regulate the harmonic distortion of the utility grid.

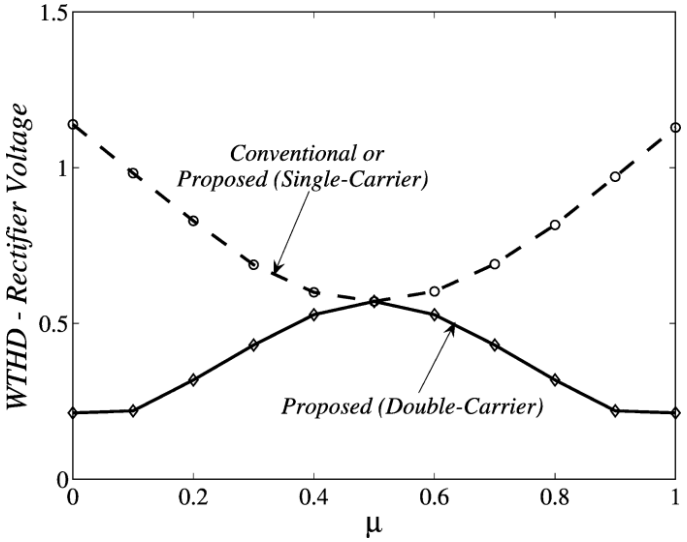

Fig. 4. *WTHD of rectifier voltage* (v_{ab} for proposed configuration and v_g for standard configuration) as a function of μ. When the single-carrier PWM is used, the behavior of *WTHD* of the proposed system is similar to that of conventional one for all μ, as observed in Fig. 4. When the double-carrier PWM is used with μ = 0.5, the *WTHD* is also the same for both configurations. However, for the other values of μ the *WTHD* of the proposed system is lower than that of the conventional one. The *WTHD* of the proposed topology (double-carrier with μ = 0or μ = 1) is close to 63% of that of the conventional topology (with μ = 0.5). The study has also shown that it is possible to reduce the switching frequency of the proposed system in 60% and still have the same *WTHD* of the standard configuration. The *WTHD* behavior in Fig. 4 can be explained from Fig. 5. That figure depicts the pole voltages ($v_{a10}, v_{a20}, v_{b10}$ **and** v_{b20}) and their references ($v^*_{a10}, v^*_{a20}, v^*_{b10}, v^*_{b20}$),the triangular carrier signals (v_{t1}, v_{t2}),the resultant rectifier voltage (v_{ab})and the circulating voltage (v_o). Fig. 5(a) and (c) shows these variables with single-carrier (with μ = 1) and double-carrier (with μ =1), respectively. For the double-carrier [see Fig.5(c)] the voltage v_{ab} has smaller amplitude and better distribution along the half switching period than that of single-carrier [see Fig. 5(a)], which means a lower *WTHD* (as observed in Fig. 4 for μs = 1). On the other hand, for μ = 0.5 [see Fig. 5(b) and (d)] the distribution of voltage v_{ab} along the switching period is the same for both cases, i.e., single-carrier and double-carrier have the same *WTHD* (as observed in Fig. 4 for μ = 0.5).

Besides the total harmonic distortion (*THD*) of the grid current i_g, associated to the *WTHD* of the voltage v_{ab}, the harmonic distortion analysis must also consider the currents in the rectifiers. This is an important issue due to losses of the converter [39], [40]. The harmonic distortion of the rectifier currents (= i_a, i_a^1, i_b, i_b^1)with double-carrier is higher than that of the grid current i_g . When the parallel rectifier with double-carrier is used, the *THD* of all these currents are reduced for μ = 0 orμ = 1 and increased for μ = 0.5. On the other hand, the *THD* of the circulating current is also smaller with μ = 0 or μ = 1. Fig. 6 shows currents i_a, i_a^1 and i_0 for double-carrier with μ = 1 and μ = 0.5. It can be seen that the mean values of the ripples of all currents are smaller when μ = 1 is selected. In conclusion,

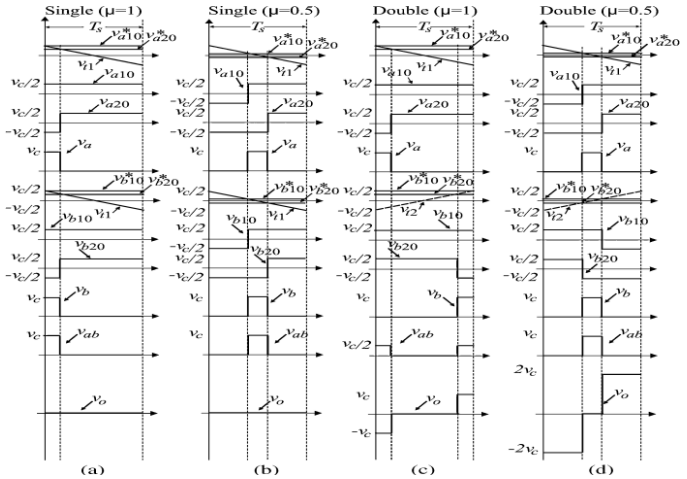

Fig. 5. Variables of rectifiers A and B. (a) Single-carrier with μ = 1. (b) Single-carrier with μ = 0.5. (c) Double-carrier with μ = 1. (d) Doublecarrier with μ = 0.5.

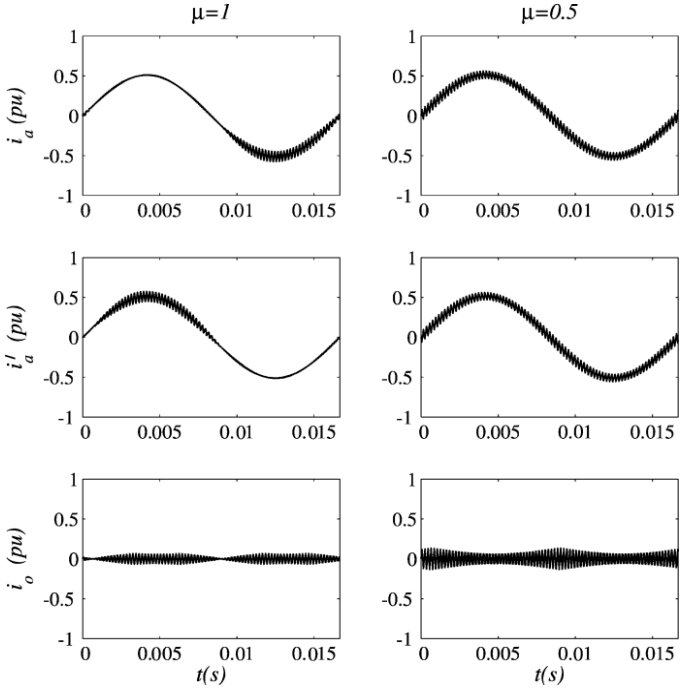

Fig. 6. Currents i_a, i_a^1 and i_0 for double-carrier with μ = 1 and μ = 0.5.

the optimal rectifier operation is obtained with double-carrier making μ = 0 or μ = 1. A four-carrier approach may

also be used. Compared with the two-carrier strategy, the four-carrier Strategy permits to reduce the harmonic distortion of the grid Current, but increases the rectifier losses.

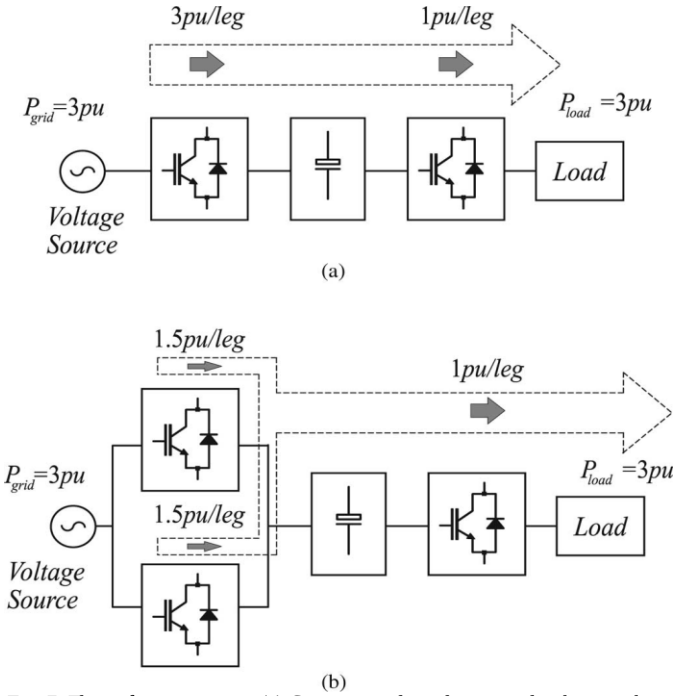

Fig. 7. Flow of active power. (a) Conventional ac–dc–ac single-phase to three phases Converter. (b) Proposed system with two rectifiers.

VI. RATINGS OF SWITCHES

Assuming same rms voltages at both grid and machine sides, a machine power factor of 0.85 and neglecting the converter losses, currents of the rectifier switches normalized in terms of currents of the inverter switches are 2.55 and 1.27 for the conventional and the proposed single-phase to three-phase converter, respectively. Fig. 7(a) and (b) shows the flow of active power in the conventional and in the proposed single-phase to three-phase converter, respectively. For balanced system ($L_g^1 = L_a = L_a^1 = L_b = L_b^1$). Voltage v_o is close to zero, so that the dc-link voltage is equal to that required by the conventional system. Since the parallel connection scheme permits to reduce the switch currents and preserve the dc-link voltage, the rating of each power switch in the rectifier side is reduced.

VII. DC-LINK CAPACITOR

The dc-link capacitor current behavior is examined in this Section. Fig. 8 illustrates the harmonic spectrums of the dc-link capacitor current for the conventional converter (μ = 0.5) [see Fig. 8(a)] and for the proposed converter using single-carrier with μ = 0.5 [see Fig. 8(b)], double-carrier with μ = 0.5 [seeFig.8(c)] and double-carrier with μ = 0 [see Fig. 8(d)]. The proposed converter using double-carrier with μ = 0 provides the best reduction of the high frequency harmonics. Table I (obtained from Fig. 8) presents the *THD* of the dc-link capacitor current of the proposed converter (THD_P) referred to the *THD* of the conventional converter (THD_C). The highest reduction of *THD* is obtained for the converter using double-carrier with μ = 0. The *THD* obtained for μ = 1 is equal to that for μ = 0.

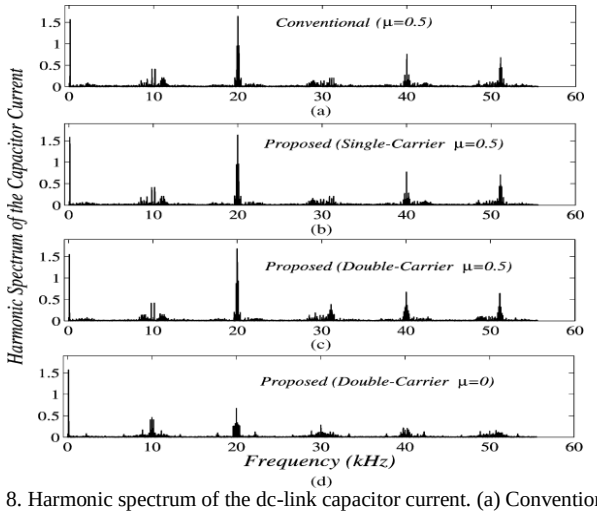

Fig. 8. Harmonic spectrum of the dc-link capacitor current. (a) Conventional converter (μ = 0.5). (b) Proposed converter with single-carrier (μ = 0.5). (c) Proposed converter with double-carrier (μ = 0.5). (d) Proposed converter with double-carrier (μ = 0).

TABLE I

NORMALIZED THD OF DC-LINK CURRENT OF THE PROPOSED CONVERTER

Topology (PWM)	$THDp/THDc$
Proposed (Single $\mu = 0.5$)	0.994
Proposed (Double $\mu = 0.5$)	1.002
Proposed (Double $\mu = 0$)	0.717

It is possible to reduce the second order harmonic introduced by single-phase operation, but this is not of interest because it requires unbalancing and increasing rectifier currents i_a and i_b.

VIII. INPUT INDUCTORS

The PWM with double-carrier strategy reduces the *WTHD* of The resultant rectifier voltage v_{ab} , as observed in Fig. 4. When the input inductors of the proposed topology (L_g^1) are equal to that of the conventional topology (L_g), the reduction of the *THD* of the grid current is directly indicated in Fig. 4.

Fig. 9 depicts the *THD* of the grid current as a function of

μ For different values of l_n [the inductances of rectifiers A and B (l_g^1) referred to that of the conventional configuration (l_g), i.e., $l_n = \frac{l_g^1}{l_g}$]. For $l_n > 0.4 (l_g^1 > 0.4 l_g)$ the *THD* of the grid current of the proposed topology is smaller than that of the conventional topology. The harmonic distortion of the rectifier currents i_a, i_a^1, i_b, i_b^1 and i_0 is higher than that of the grid current i_g. The adequate choice of the PWM strategy permits to operate with minimum harmonic distortion. We have considered the losses as the main

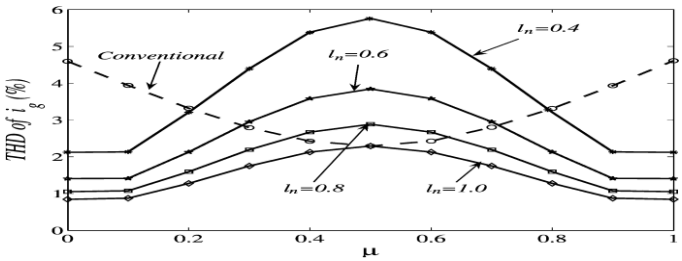

Fig. 9. Inductor specification in terms of *THD* of i_g and μ

Concern to define the maximum acceptable harmonic distortion of the rectifier currents (see Section X). In any case, the use of additional common-mode inductors is a very efficient manner of reduces the harmonic distortion of these currents [12]. This approach may be also employed in the present case to reduce the total inductance required for an adequate operation of the system.

The design of inductors may follows the guide lines presented in [12] for an active power filter system.

IX. FAULT COMPENSATION

The proposed system presents redundancy of the rectifier converter, which can be useful in fault-tolerant systems. The proposed system can provide compensation for open-circuit and short-circuit failures occurring in the rectifier or inverter converter devices.

The fault compensation is achieved by reconfiguring the power converter topology with the help of isolating devices (fast active fuses—F_j, j=1, . . . , 7) and connecting devices (back to- back connected SCRs—*t*1 , *t*2 , *t*3), as observed in Fig. 10(a) and discussed in [41]–[44]. These devices are used to redefine the post-fault converter topology, which allows continuous operation of the drive after isolation of the faulty power switches in the converter. Fig. 10(b) presents the block diagram of the fault diagnosis system. In this figure, the block fault identification system (FIS) detects and locates the faulty switches, defining the leg to be isolated. This control system is based on the analysis of the pole voltage error.

The fault detection and identification is carried out in four steps:

1) measurement of pole voltages(v_{j0});
2) computation of the voltage error ϵ_{J0} by comparison of reference voltages and measurements affected in Step 1);
3) Determination as to whether these errors correspond or not to a faulty condition; this can be implemented by the hysteresis detector shown in Fig. 10(b);
4) Identification of the faulty switches by using $\epsilon^1_{JO.}$

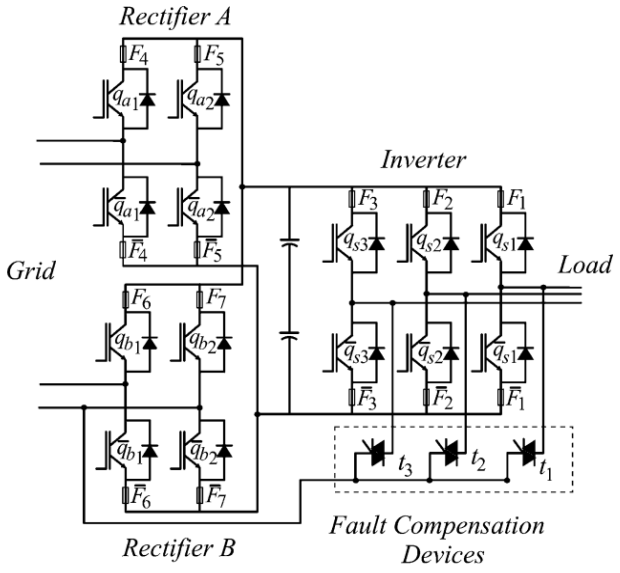

Fig. 10. (a) Proposed configuration highlighting devices of fault-tolerant system. (b) Block diagram of the fault diagnosis system.

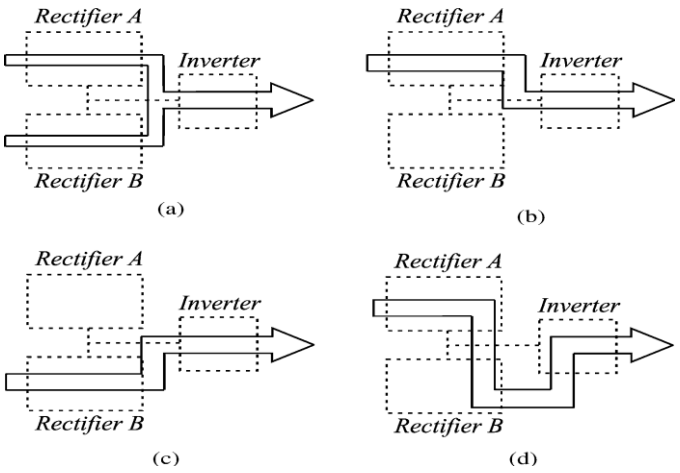

Fig. 11. Possibilities of configurations in terms of fault occurrence. (a) Prefault system. (b) Post-fault system with fault at the rectifier B. (c) Post-fault system with fault at the rectifier A. (d) Post-fault system with fault at the inverter.

This way, four possibilities of configurations have been considered in terms of faults:
1) *Pre-fault* ("healthy") operation [see Fig. 11(a)];
2) *Post-fault* operation with fault at the rectifier B [see Fig. 11(b)];

TABLE III

EFFICIENCY OF THE PROPOSED SYSTEM NORMALIZED IN TERMS CONVENTIONAL ONE:

$(\eta_p/\eta_c - 1)$			
Frequency/Inductor	S-Ca $\mu = 0.5$	D-Ca $\mu = 0.5$	D-Ca $\mu = 0$
$10kHz/(L_g^{'} = L_g)$	-1.60%	-1.47%	-0.41%
$10kHz/(L_g^{'} = L_g/2)$	3.12%	3.25%	4.36%
$5kHz/(L_g^{'} = L_g)$	-0.74%	-0.27%	1.72%

3*) Post-fault* operation with fault at the rectifier A [see Fig. 11(c)];
4) *Post-fault* operation with fault at the inverter [see Fig. 11(d)].

When the fault occurrence is detected and identified by the control system, the proposed system is reconfigured and becomes similar to that in Fig. 1. For instance, if a fault in any switch of rectifier A has been detected by the control system, the whole rectifier needs to be isolated. This isolation procedure depends on the kind of fault detected. If an open-circuit failure is detected, the control system will open all switches of the rectifier A. On the other hand, if a short circuit is detected, the control system will turn on all switches related to rectifier A, and in this case, the fuses will open, and consequently, the rectifier will be isolated, as discussed in [41]–[44]. Considering now a fault in one leg of inverter, in this case the SCR related with this leg in turned on and the leg $b1$ is isolated, so that the leg $b2$ of rectifier B will operate as the leg of inverter.

X. LOSSES AND EFFICIENCY

The evaluation of the rectifier losses is obtained through regression model presented in [45]. The switch loss model includes: 1) IGBT and diode conduction losses; 2) IGBT turn-ON losses; 3) IGBT turn-OFF losses; and 4) diode turn-OFF energy. The loss evaluation takes into account just the rectifier circuit, since the inverter side of converter is the same for the proposed and standard configurations.

When the rectifiers operate with a switching frequency equal to 5 kHz, the conduction and switching losses of the proposed topology were 70% and 105%, respectively, of the corresponding losses of the conventional topology. Consequently, in this case, the total losses of the proposed topology were smaller than that of the conventional topology. The increase of the switching frequency does not change the conduction losses of both topologies, but increases their switching losses, especially for the proposed topology that has a high number of switches.

The efficiency of the topologies operating with a switching Frequency equal to 10 kHz and 5 kHz was evaluated by Experimental measurement with a 2 kW load. Table II shows the experimental results of the rectifier efficiency. Such results are obtained for the proposed system (η_p) normalized in terms conventional one (η_c), for three cases: 1) both rectifiers operating at 10 kHz and $L_g^1 = L_g$; 2) both rectifiers operating at 10 kHz and $L_g^1 = L_g/2$; and 3) both rectifiers operating at5 kHz and $L_g^1 = L_g$. Three strategies are considered in terms of PWM control: 1) single-carrier with μ= 0.5 (S-Ca μ = 0.5); 2) double-carrier with μ = 0.5 (D-Ca μ = 0.5); and 3) double carrier with μ = 0 (D-Ca μ = 0). For case 1) the proposed configuration with double-carrier and μ = 0 have its efficiency slightly smaller than that of the conventional one, but with the other PWM strategies its efficiency is clearly inferior. In the other cases, the proposed configuration with double-carrier and μ = 0 presents higher efficiency than the conventional one.

XI. SIMULATION RESULTS

The system shown in Fig. 2 has been implemented in the laboratory. The setup used in the experimental tests is based on a microcomputer equipped with appropriate plug-in boards and sensors. The system operates with a switching frequency equal to 10 kHz. Steady state, transient, fault analysis, and interleave operation have been evaluated in the experimental testes.

The steady-state experimental results are shown in Fig. 12. The waveforms in this figure are: (a) voltage and current of the grid, (b) dc-link voltage, (c) currents of rectifier A and circulating current, (d) currents of rectifiers A and B, and (e) load line voltage. Note that, with the proposed configuration, All control demanded for single-phase to three-phase converter
has been established. The control guarantees sinusoidal grid current with power factor close to one [see Fig. 12(a)], dc-link and machine voltages under control [see Fig. 12(b) and (e)]. Furthermore, the proposed configuration provides current reduction in the rectifier side (half of the current of the standard topology) [see Fig. 12(d)], which can provide loss reduction. Also, the control guarantees the circulating current close to zero [see Fig. 12(c)].

The same set of experimental results was obtained for transient in the machine voltages, as observed in Fig. 13. A volts/hertz control was applied for the three-phase machine, From V/Hz = 83.3 V/40 Hz to V/Hz = 125 V/60 Hz [see Fig. 13(e)], which implies in increased of power furnished by the grid [see Fig. 13(a)]. In spite of this transient, the dc-link Voltage [see Fig. 13(b)] and other variables are under control [see Fig. 13(c) and (d)].

Experimental results presented in Fig. 14 show the behavior of variables of the proposed system when a fault is detected in rectifier B. In this case, after fault detection given by the control system, the rectifier B has been isolated and the total flux of energy flows through rectifier A. Fig. 14 shows grid voltage and current, currents of rectifiers A and B, capacitor voltage, and currents of rectifier A. The fault occurrence is intentionally created by using bypass switches.

Fig. 15 shows the effect of interleaved operation in terms of grid and converter currents, i.e i_g , i_a and i_b . Point 1 of Fig. 15(a) indicates these variables (i_g , i_a and i_b) when they flow at their peak values, as highlighted in Fig. 15(b). Instead, point 2 of Fig. 15(a) shows the current when they cross the zero, as highlighted in Fig. 15(c). Note that the benefit of the interleaved operation is emphasized in point 2, when the voltage pulse pattern has a duty cycle close to 0.5.

XII. CONCLUSION

A single-phase to three-phase drive system composed of two parallel single-phase rectifiers, a three-phase inverter and an induction motor was proposed. The system combines two parallel rectifiers without the use of transformers. The system model and the Fuzzy control strategy, including the PWM technique, have been developed.

The complete comparison between the proposed and standard Configurations have been carried out in this paper. Compared to the conventional topology, the proposed system permits to Reduce the rectifier switch currents, the *THD* of the grid current with same switching frequency or the switching frequency with same *THD* of the grid current and to increase the fault tolerance characteristics. In addition, the losses of the proposed system may be lower than that of the conventional counterpart.

The initial investment of the proposed system (due to high number of semiconductor devices) cannot be considered a drawback, especially considering the scenario where the cited advantages justify such initial investment.

The simulation results have shown that the system is controlled properly, even with transient and occurrence of faults.

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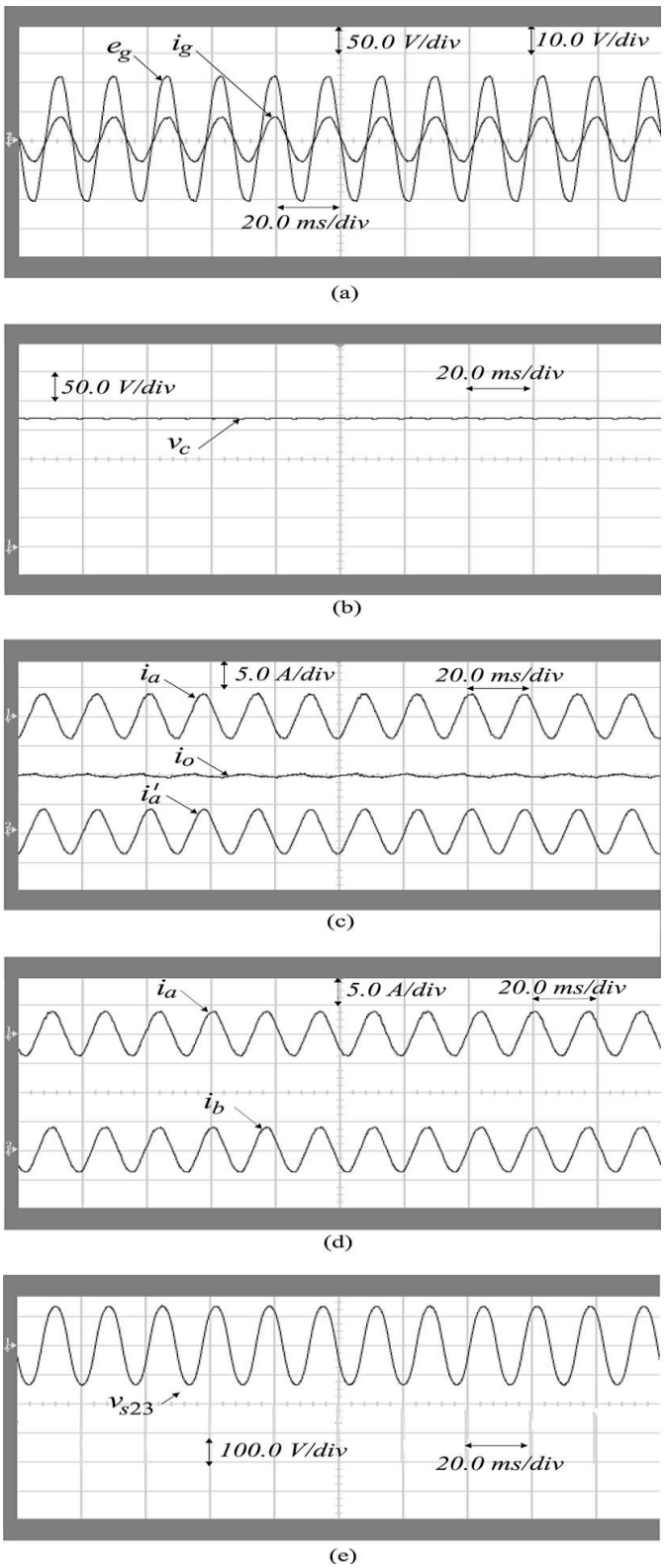

Fig.12.steady-State Simulation Results.(a)Grid Voltage(Eg) And Grid Current (ig) ,(b) Capacitor Voltage (Vc), (c) Current of Rectifier A(ia) and B(ib),(e) Line Voltage of the load(V23).

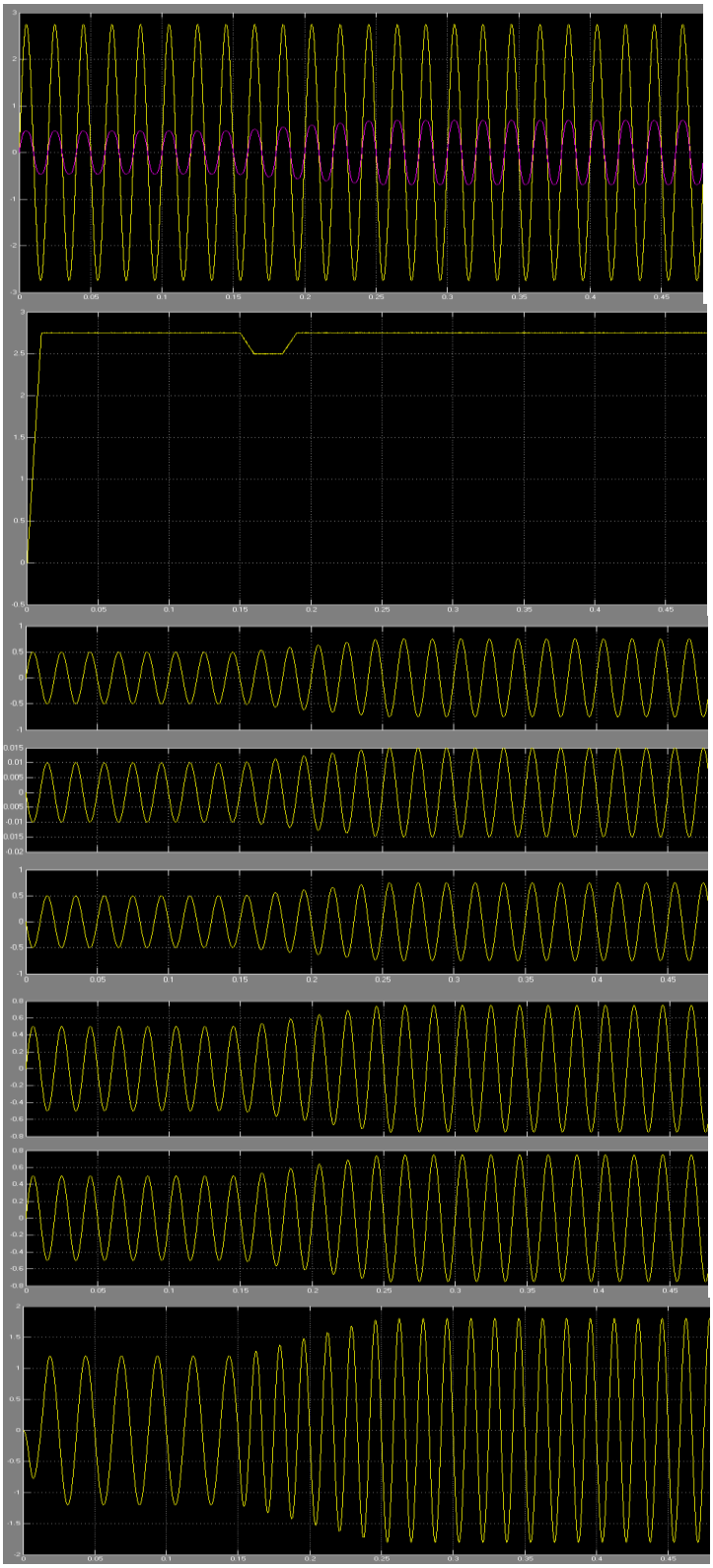

Fig.13 .Simulation Results Grid voltage and current Capacitor voltage (Vc) Current of rectifier A and circulating current Current of rectifier A and B Line voltage of the load.

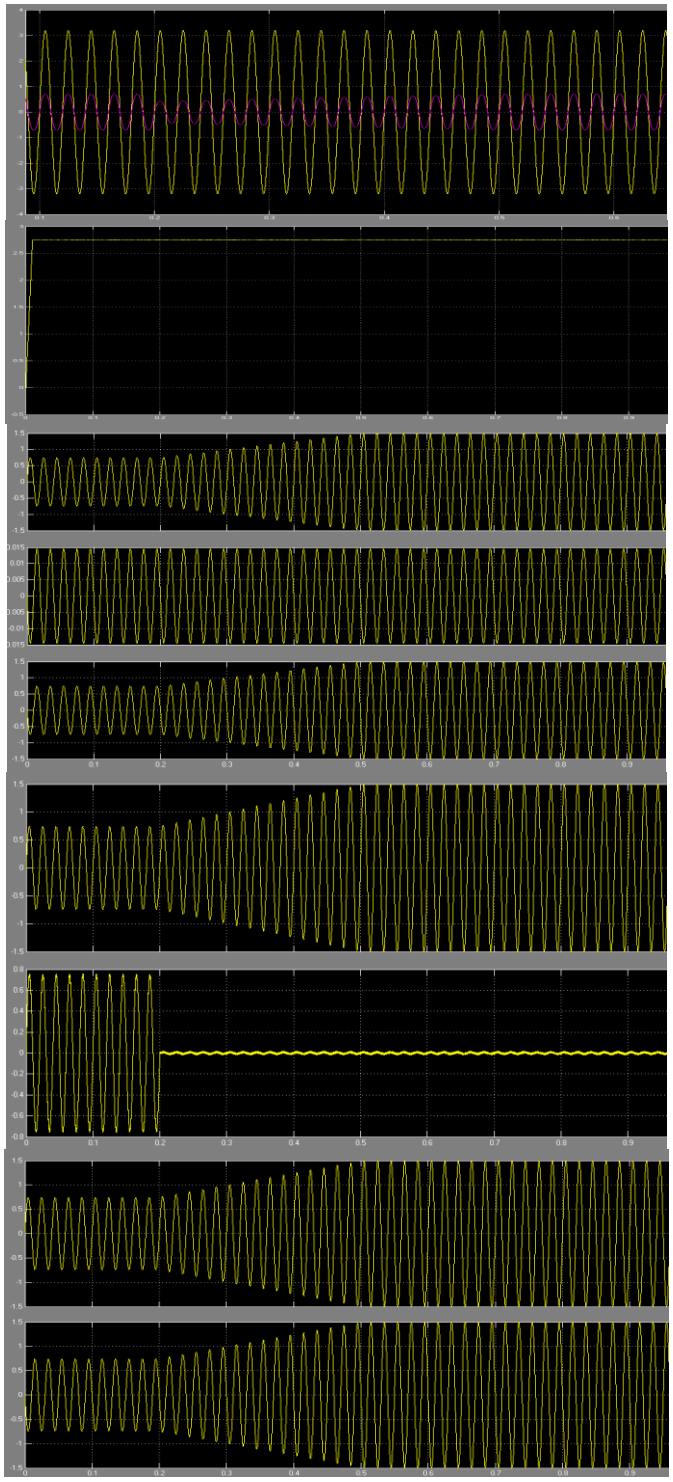

Fig.14.Grid voltage and grid current, Capacitor voltage (Vc) ,Current wave forms, Current of rectifier A and B, Currents of rectifier A with fuzzy controller.

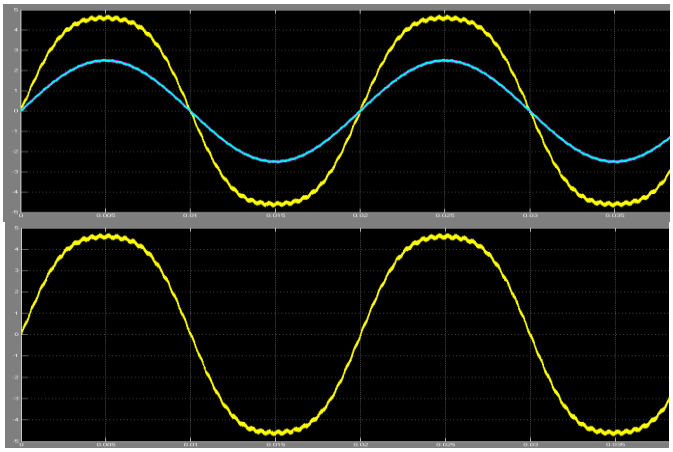

Fig.15.Grid current (Ig) and current of rectifier A and B, Grid current (Ig).

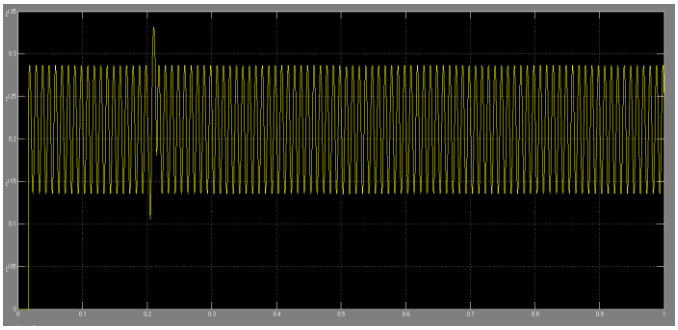

Fig.16.total harmonic distortion in pi controller (THD in pi controllers 33 percentage).

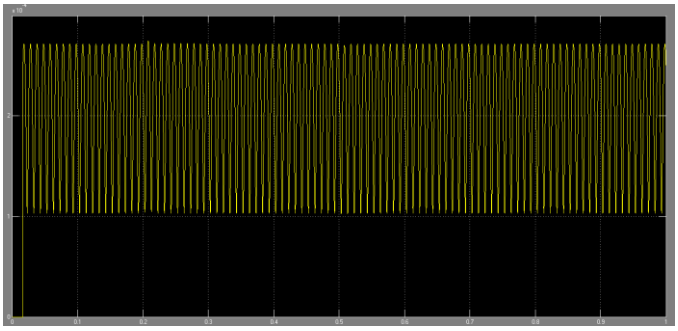

Fig.17.total harmonic distortion in fuzzy logic controller (THD is 0.04 percentage means totally minimize the system errors).

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